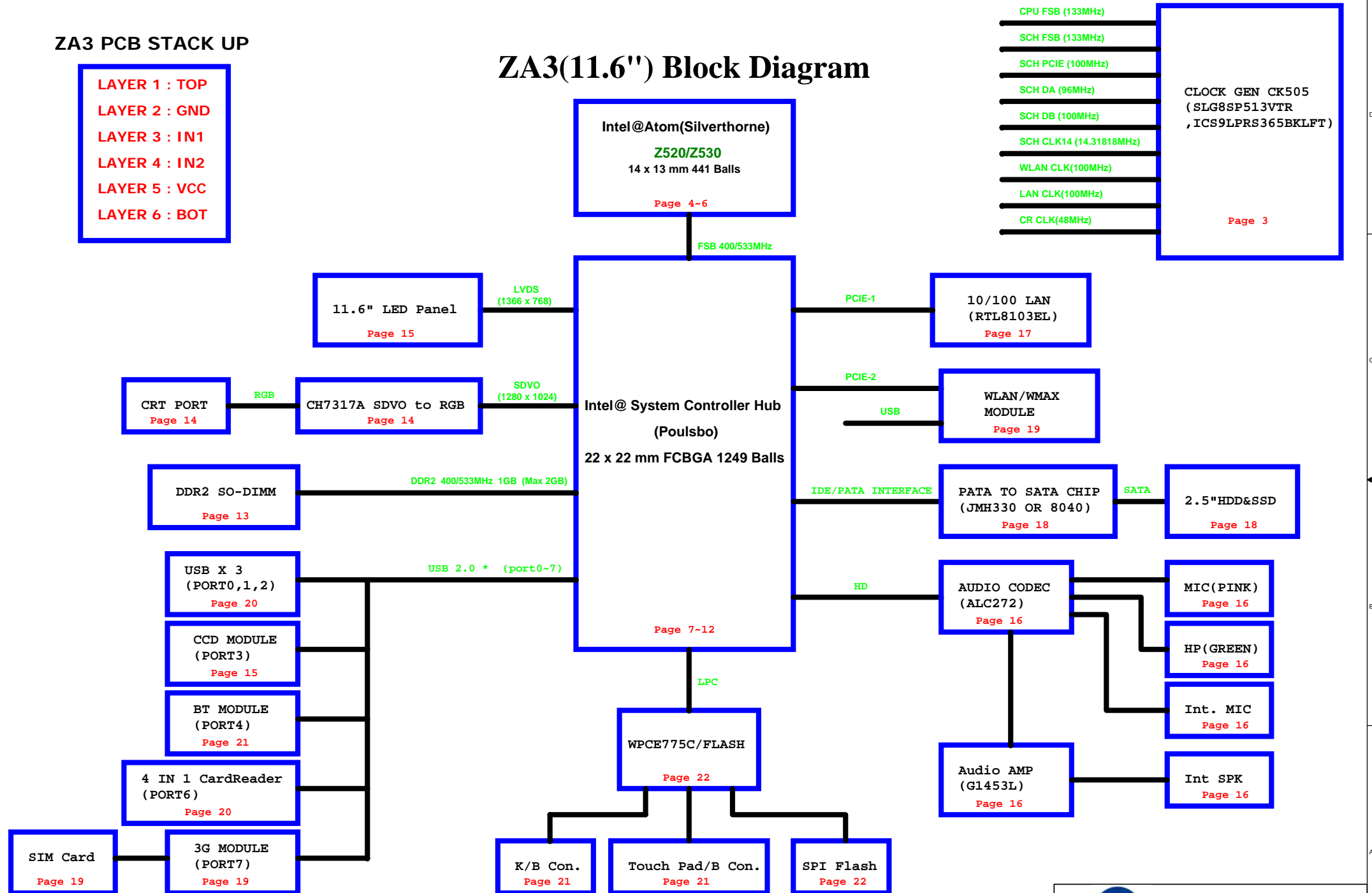


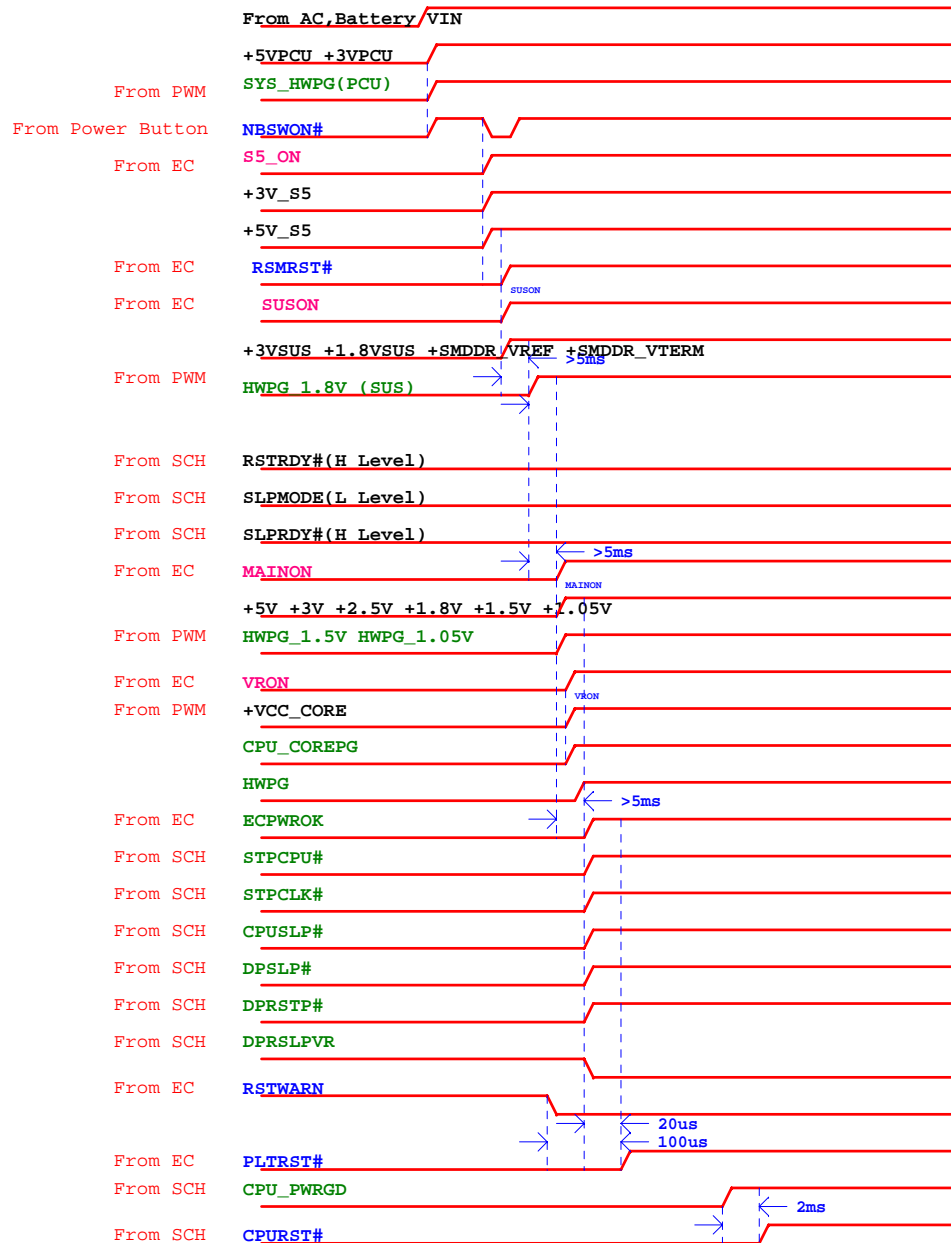
## ZA3 PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

## ZA3(11.6") Block Diagram



## ZA3 Power On Sequence



## BOM naming rule

Items	Function	Name	Description
1	PATA TO SATA BRIDGE	8040@	Marvell 88SE8040
2	PATA TO SATA BRIDGE	330@	Jmicron JMH330
3	3G Module	3G@	
4	FAN Module	FAN_PWM@	PWM FAN
5			
6			

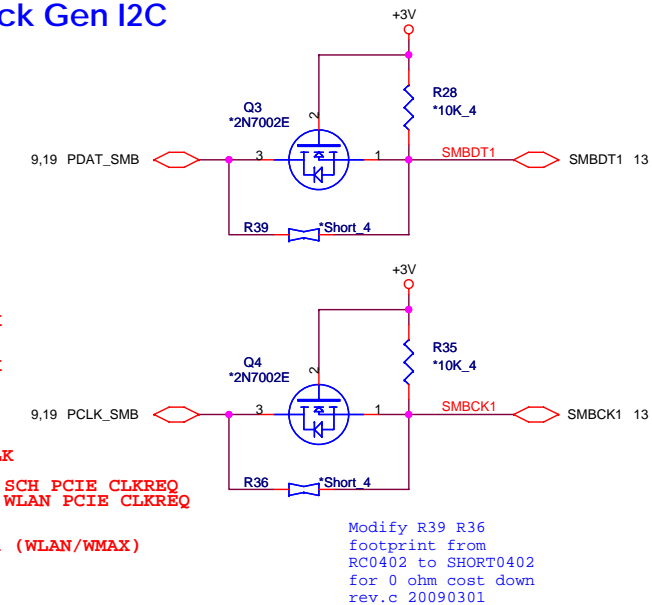
## Poulsbo SCH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN/WMAX)	Mini Card (3G)
(SMB_DATA) / (SMB_CLK) (+3V)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3VSUS
MOS CKT	Reserve	Reserve	Reserve	Reserve

## EC SMBUS Table

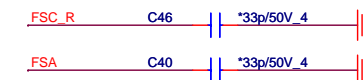
	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDA1 / SCL1 (+3VPCU)	V		
EC775 SDA2 / SCL2 (+3VPCU)		V	V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	Stuff	X

## Clock Gen I2C



Modify R39 R36  
footprint from  
RC0402 to SHORT0402  
for 0 ohm cost down  
rev.c 20090301

EMI



The schematic shows three differential input pairs for the ADXL345. Each pair is connected to a +3V supply and ground. The resistors are labeled R34, R33, R32, R31, R30, and R29, with values of 10K 4 and \*10K 4. The inputs are labeled PCI2, PCI4, and PCI6.

PCI\_STOP#  
PM\_STPCPU#

—○ +3V

SCM\_BSEL2 7

GPU\_BSEL2 5

1. *Chlorophyll a* (Chl a) is the primary photosynthetic pigment in most plants and algae. It is a green pigment that absorbs light energy in the blue and red regions of the visible spectrum. Chl a is essential for the light-dependent reactions of photosynthesis, where it converts light energy into chemical energy in the form of ATP and NADPH.

change the  $\gamma$  from

CS31002JB28  
rev. c 20090301

---

2

CLK GEN &amp; PWR

25 VR\_PWRGD\_CK410#



ange R43 P/N

0002JB38 to  
1002JB28

20090501

2

FSC	FSB	FSA	CPU	SRC	PCI	States
1	0	1	100	100	33	
0	0	1	133	100	33	Default

Change R43 P/N  
from  
CS00002JB38 to  
CS31002JB28  
rev.c 20090301



**Quanta Computer Inc.**

PROJECT : ZA3

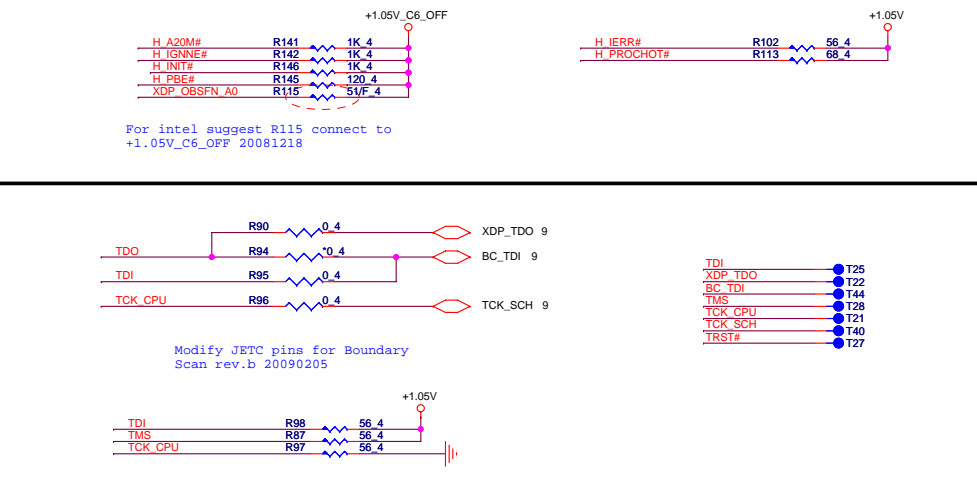
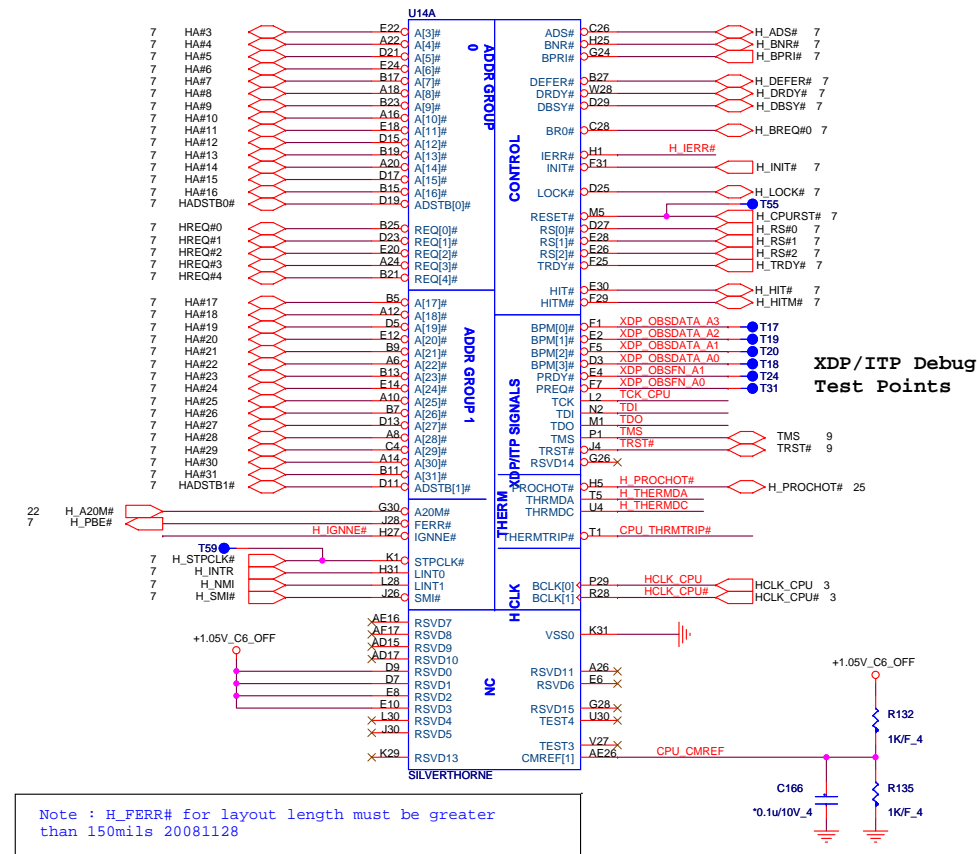
Size	Document Number	Rev
	<b>CLOCK GEN(CK505)</b>	1A
Date:	Sunday, March 08, 2009	Sheet 3 of 34

Date: Sunday, March 08, 2009 Sheet 3 of 34

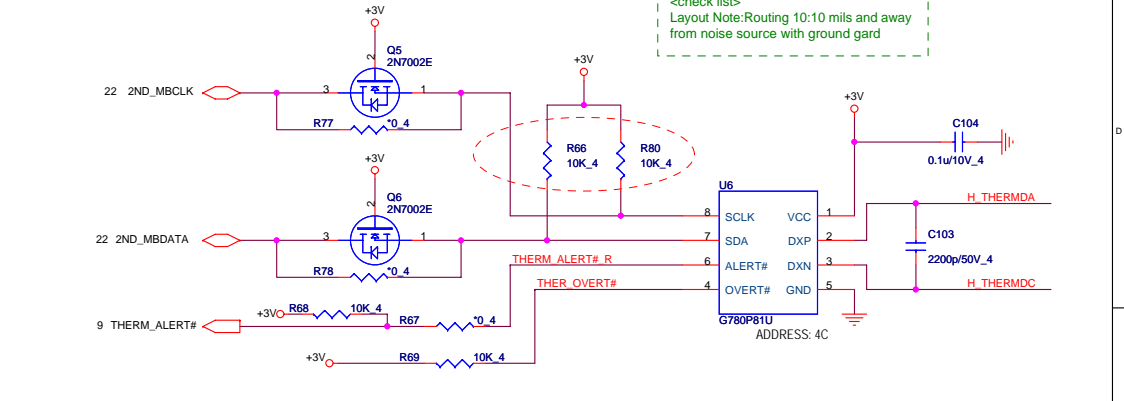
Date: Sunday, March 08, 2009 Sheet 3 of 34

Date: Sunday, March 08, 2009 Sheet 3 of 34

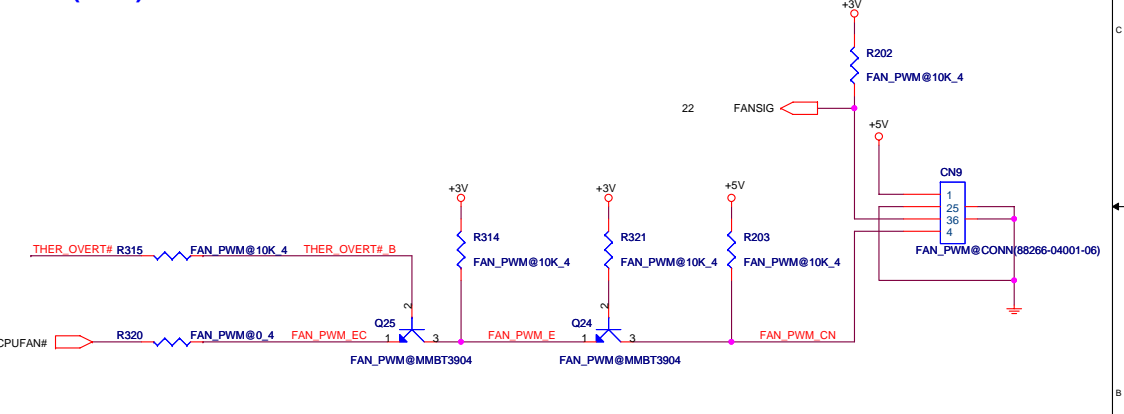
Silverthorne(CPU)



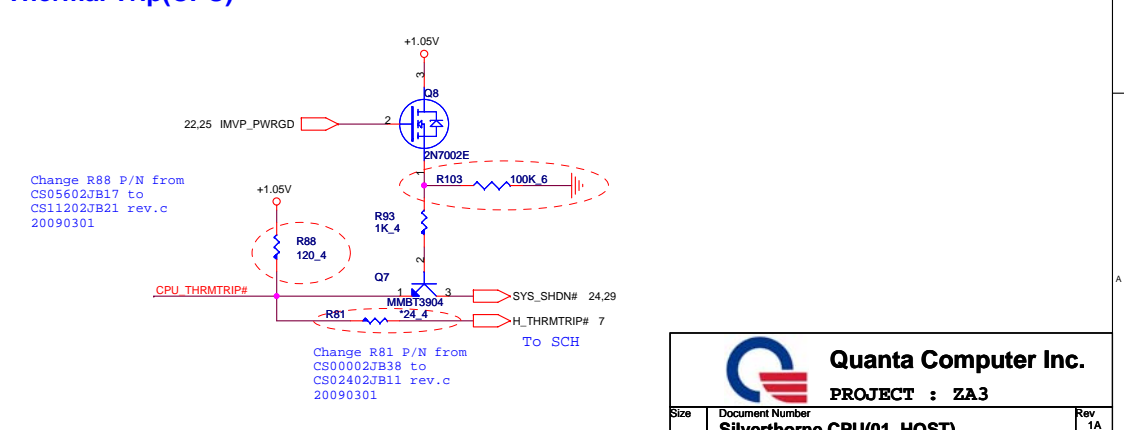
CPU Thermal monitor(THM)




FAN(THM)



Thermal Trip(CPU)



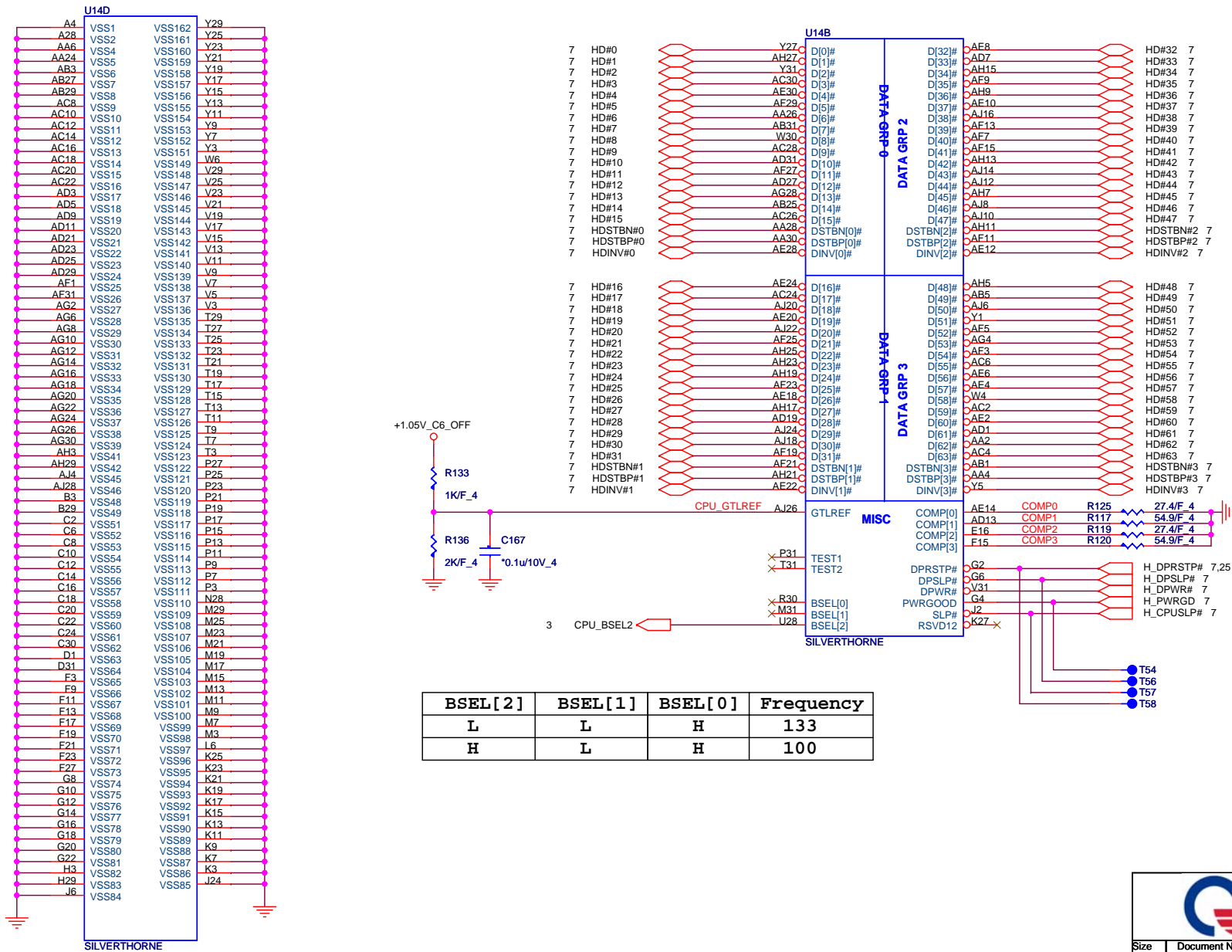


**Quanta Computer Inc.**

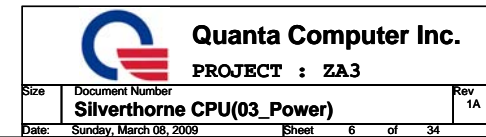
**PROJECT : ZA3**

Size	Document Number	Rev
	<b>Silverthorne CPU(01_HOST)</b>	1A
Date:	Sunday, March 08, 2009	Sheet 4 of 34

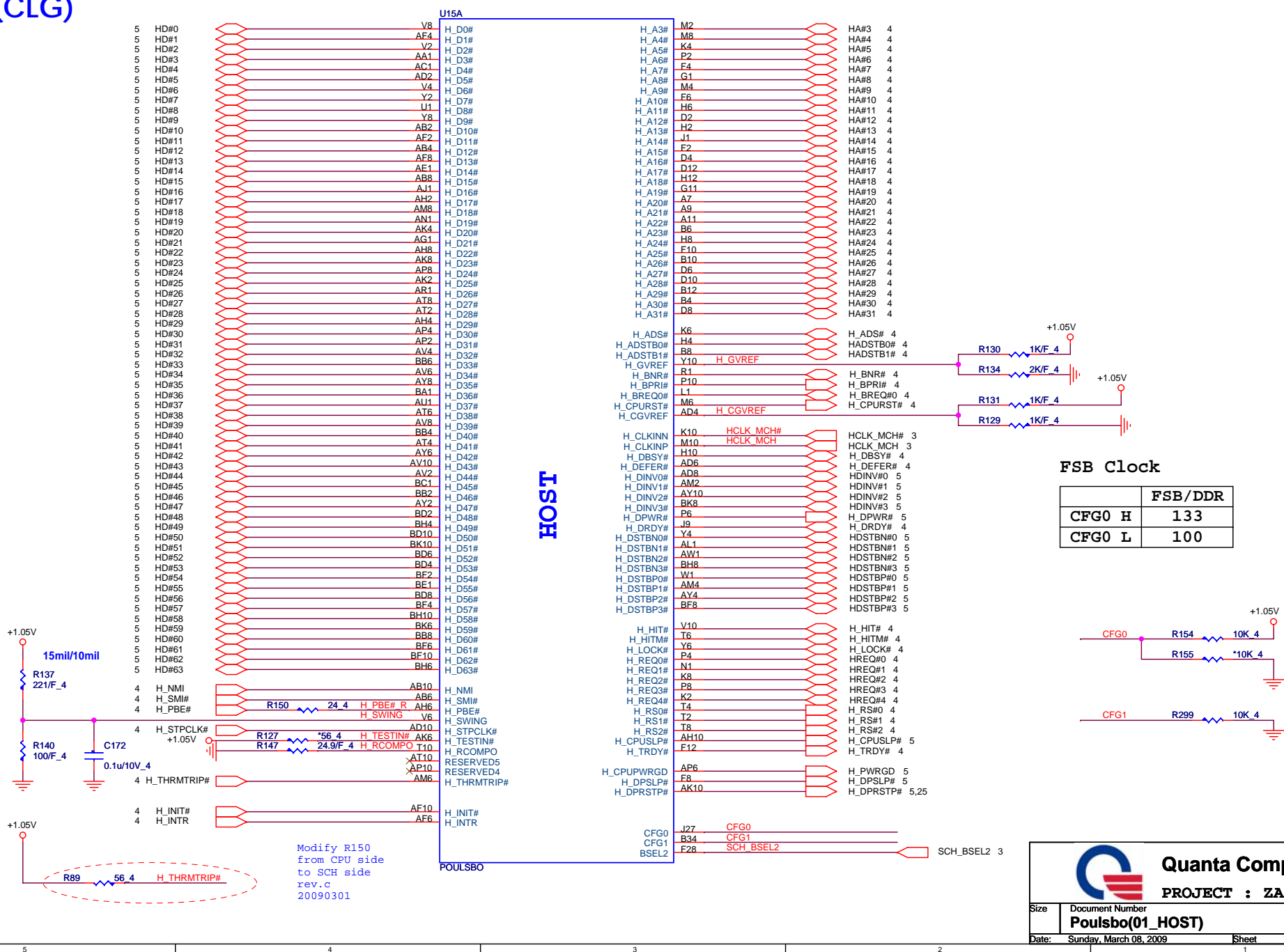
# Silverthorne(CPU)



**WWW.AliSaler.Com**




Poulsbo(CLG)



FSB Clock

	FSB/DDR
CFG0 H	133
CFG0 L	100



**Quanta Computer Inc.**  
PROJECT : ZA3

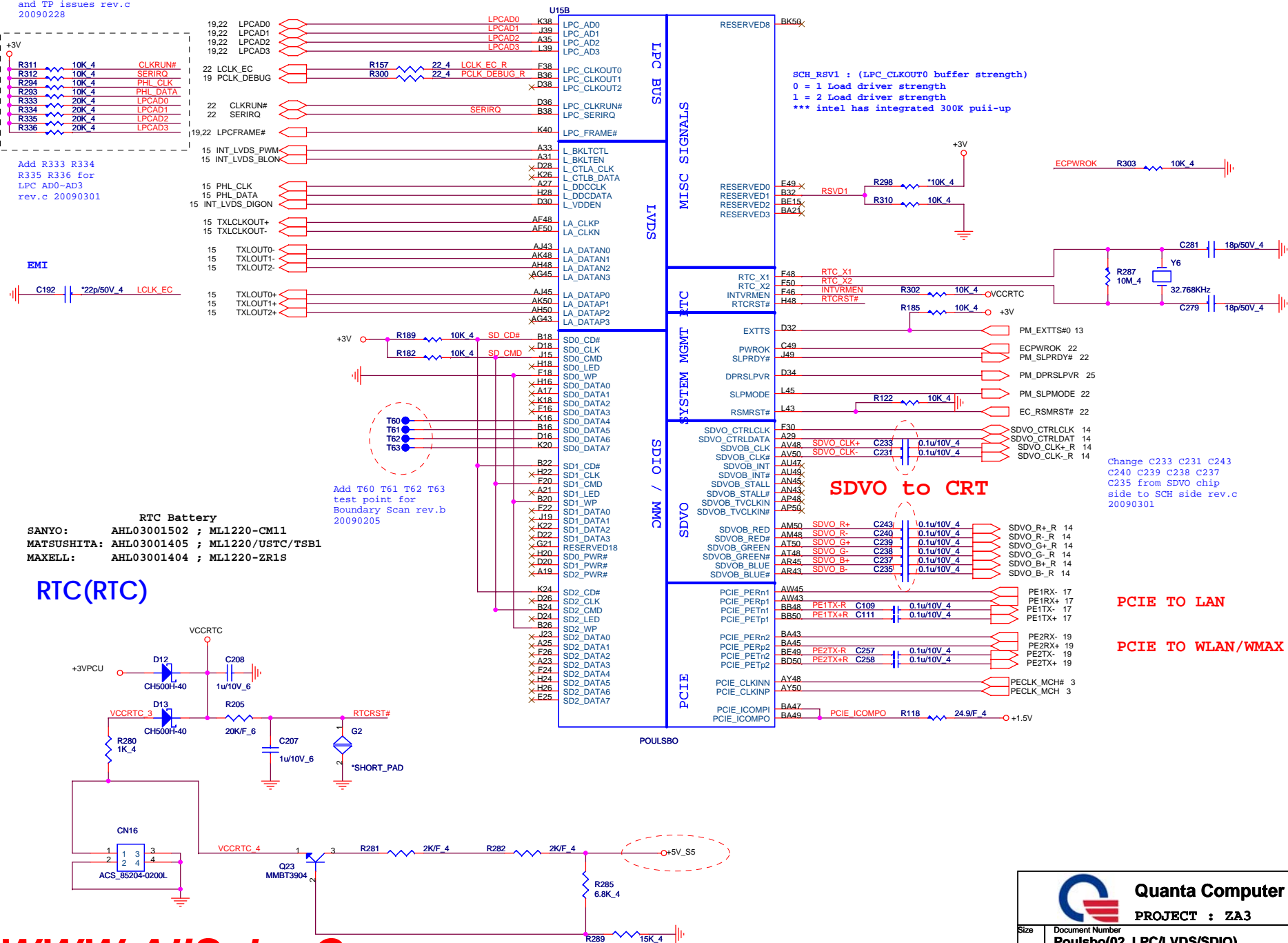
Size	Document Number	Rev
	<b>Poulsbo(01_HOST)</b>	1A
Date:	Sunday, March 08, 2009	Sheet 7 of 34

Modify R150  
from CPU side  
to SCH side  
rev.c  
20090301



## Poulsbo(CLG)

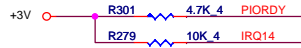
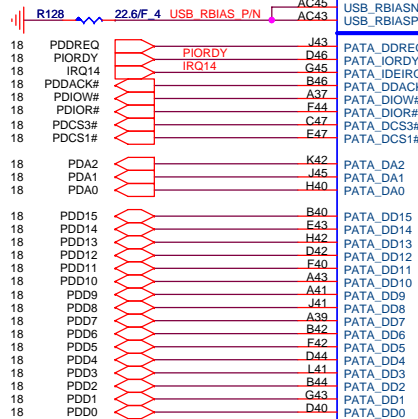
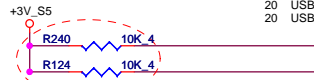
Stuff R312 for Keyboard  
and TP issues rev.c  
20090228





# Poulsbo(CLG)

- 0---MB USB PORT1
- 1---MB USB PORT2
- 2---DB USB PORT3
- 3---CCD Module
- 4---BT Module
- 5---MINI WLAN/WMAX
- 6---CARD READER
- 7---MINI 3G Module



Termination Voltage

PATA/IDE

UTAG

SYSTEM GPIOs

No-Connect

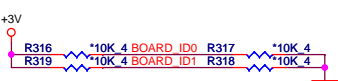
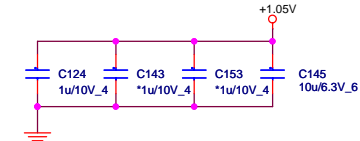
HD AUDIO

CLOCK I/F

SMB

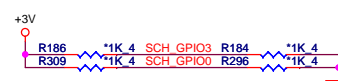
POULSBO

## XDP/ITP Debug Test Points



ID1	ID0	Functions
0	0	
0	1	
1	0	
1	1	

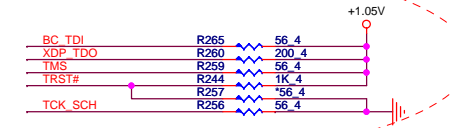
\* : Default



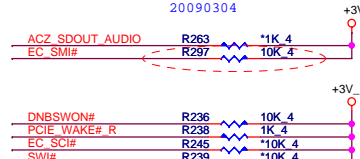
GPIO3	GPIO0	CMC Base Add.
0	0	FFFB000h
0	1	FFFC000h
1	0	FFFD000h(*)
1	1	FFFE000h

\* : Default

Modify JETC pins for Boundary Scan rev.b 20090205



Change R297 from +3V\_S5 to +3V for SMI# rev.c 20090304



For intel suggest add R295 pull down 20081218

SCH GFX Clock  
SCH GFX SS Clock

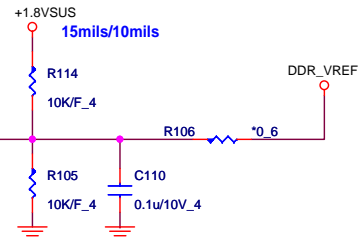
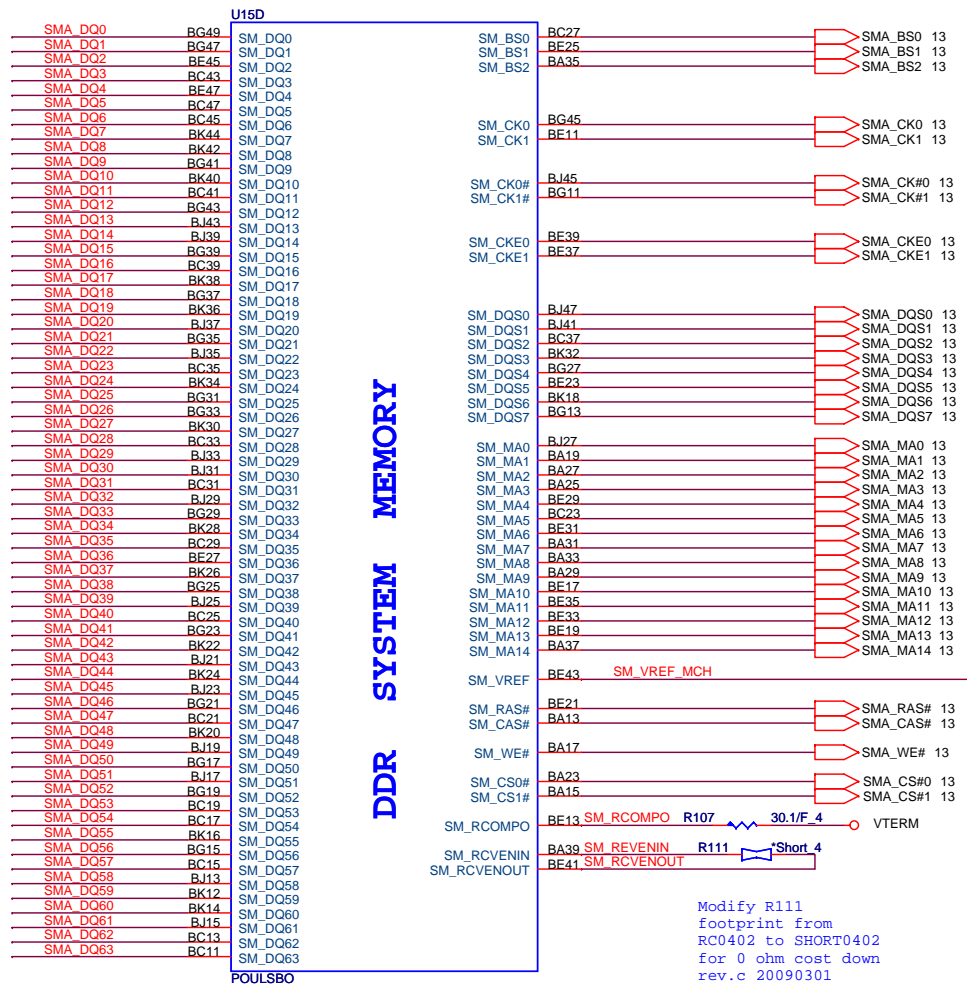
Del RN8 and Add R337 R338 to SCH SMBUS rev.c 20090301

**Quanta Computer Inc.**


**PROJECT : ZA3**

Size	Document Number	Rev
	<b>Poulsbo(03_USB/PATA/HD)</b>	1A
Date:	Sunday, March 08, 2009	Sheet 9 of 34

13 SMA\_DQ[63..0]



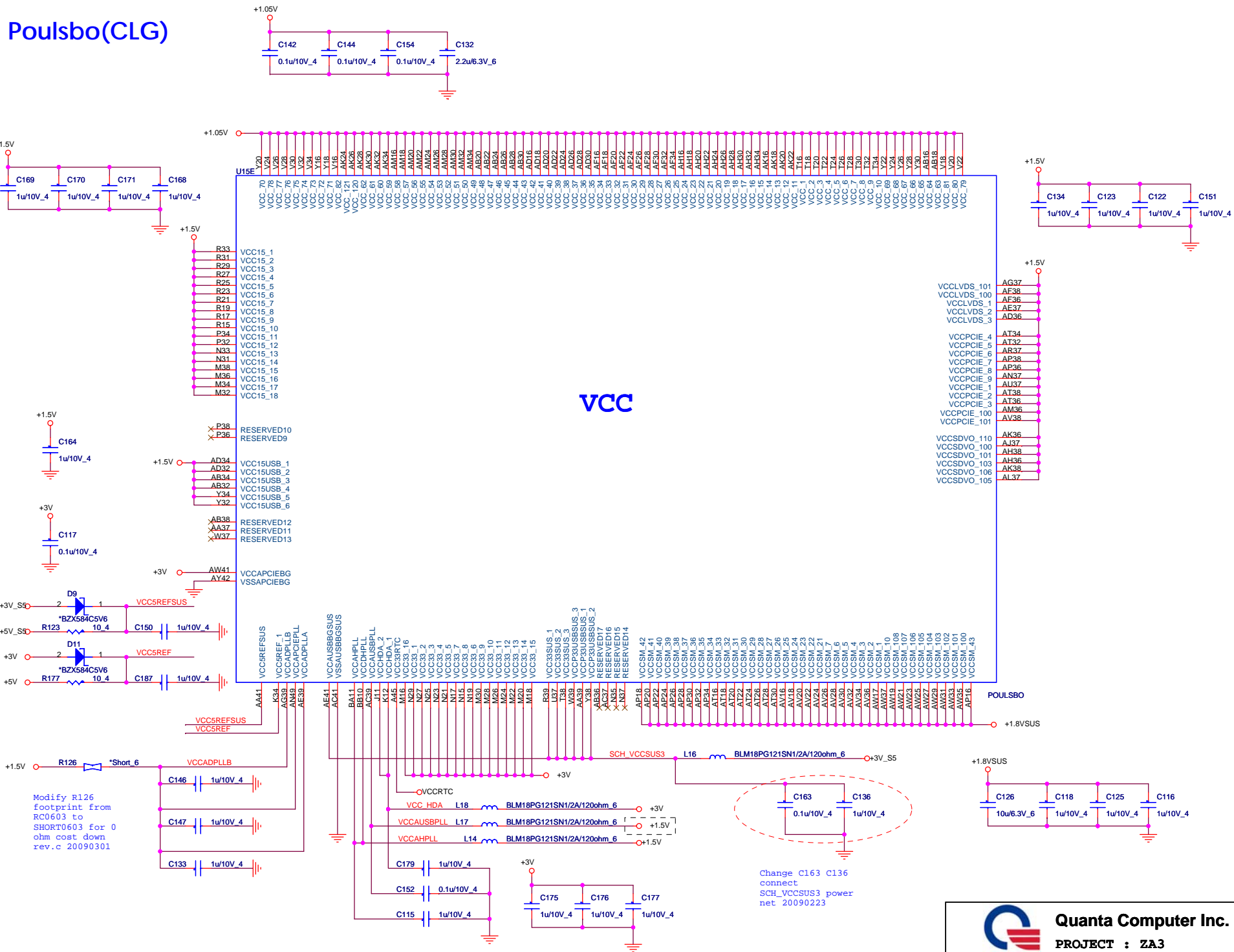
Modify R111  
footprint from  
RC0402 to SHORT0402  
for 0 ohm cost down  
rev.c 20090301



Quanta Computer Inc.  
PROJECT : ZA3

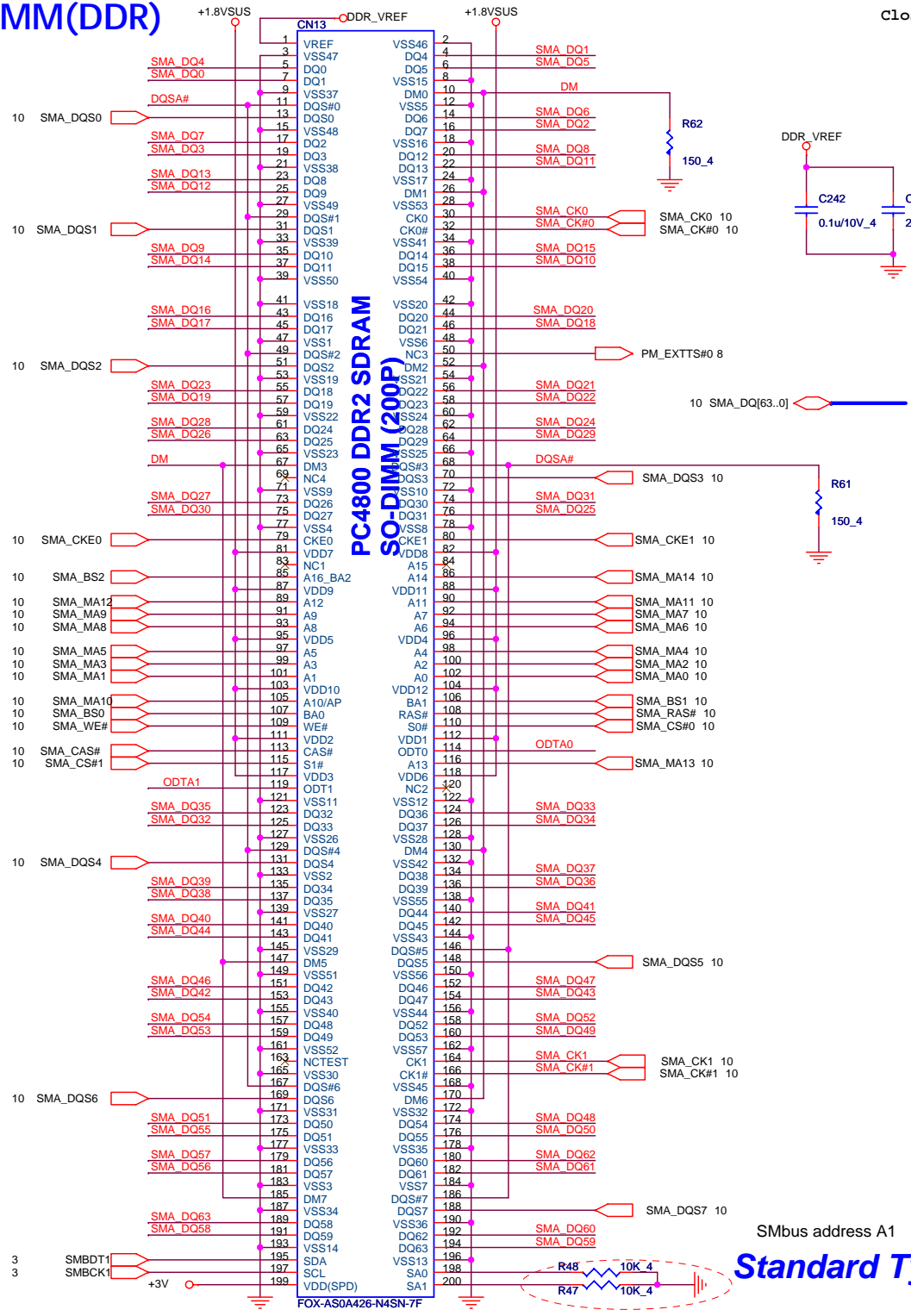
Size	Document Number	Rev
	Poulsbo(04_MEM)	1A
Date:	Sunday, March 08, 2009	Sheet 10 of 34

## Poulsbo(CLG)

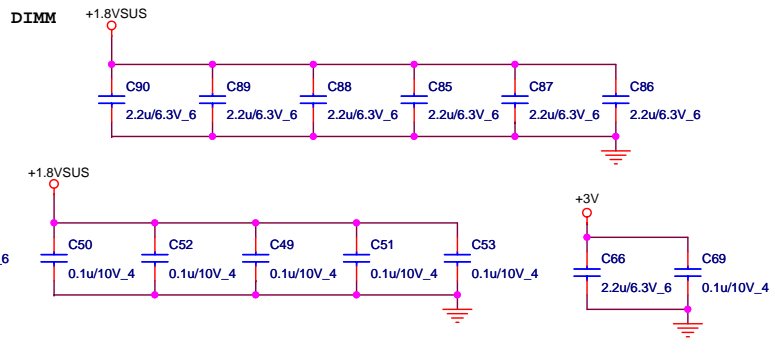



U19F			RB24		
BH30	VSS_1	VSS_76	BH22	VSS_77	BH22
BH28	VSS_2	VSS_78	BA5	VSS_84	BA7
BH26	VSS_3	VSS_85	BA6	VSS_85	BA7
BH24	VSS_4	VSS_86	BA3	VSS_86	BA7
BH22	VSS_5	VSS_87	AY46	VSS_88	AY46
BH20	VSS_6	VSS_88	AY44	VSS_89	AY44
BH18	VSS_7	VSS_89	AY40	VSS_90	AY40
BH16	VSS_8	VSS_90	AY38	VSS_91	AY38
BH14	VSS_9	VSS_91	AY36	VSS_92	AY36
BH12	VSS_10	VSS_92	AY34	VSS_93	AY34
BH10	VSS_11	VSS_93	AY32	VSS_94	AY32
BH08	VSS_12	VSS_94	AY30	VSS_95	AY30
BH06	VSS_13	VSS_95	AY28	VSS_96	AY28
BH04	VSS_14	VSS_96	AY26	VSS_97	AY26
BH02	VSS_15	VSS_97	AY24	VSS_98	AY24
BH00	VSS_16	VSS_98	AY22	VSS_99	AY22
BF50	VSS_17	VSS_99	AY18	VSS_100	AY18
BF48	VSS_18	VSS_100	AY16	VSS_101	AY16
BF46	VSS_19	VSS_101	AY14	VSS_102	AY14
BF44	VSS_20	VSS_102	AY12	VSS_103	AY12
BF42	VSS_21	VSS_103	AY10	VSS_104	AY10
BF40	VSS_22	VSS_104	AY08	VSS_105	AY08
BF38	VSS_23	VSS_105	AY06	VSS_106	AY06
BF36	VSS_24	VSS_106	AY04	VSS_107	AY04
BF34	VSS_25	VSS_107	AY02	VSS_108	AY02
BF32	VSS_26	VSS_108	AY00	VSS_109	AY00
BF30	VSS_27	VSS_109	AY00	VSS_110	AY00
BF28	VSS_28	VSS_110	AY00	VSS_111	AY00
BF26	VSS_29	VSS_111	AY00	VSS_112	AY00
BF24	VSS_30	VSS_112	AY00	VSS_113	AY00
BF22	VSS_31	VSS_113	AY00	VSS_114	AY00
BF20	VSS_32	VSS_114	AY00	VSS_115	AY00
BF18	VSS_33	VSS_115	AY00	VSS_116	AY00
BF16	VSS_34	VSS_116	AY00	VSS_117	AY00
BF14	VSS_35	VSS_117	AY00	VSS_118	AY00
BF12	VSS_36	VSS_118	AY00	VSS_119	AY00
BF10	VSS_37	VSS_119	AY00	VSS_120	AY00
BF08	VSS_38	VSS_120	AY00	VSS_121	AY00
BF06	VSS_39	VSS_121	AY00	VSS_122	AY00
BF04	VSS_40	VSS_122	AY00	VSS_123	AY00
BF02	VSS_41	VSS_123	AY00	VSS_124	AY00
BF00	VSS_42	VSS_124	AY00	VSS_125	AY00
BD46	VSS_43	VSS_125	AY00	VSS_126	AY00
BD44	VSS_44	VSS_126	AY00	VSS_127	AY00
BD42	VSS_45	VSS_127	AY00	VSS_128	AY00
BD40	VSS_46	VSS_128	AY00	VSS_129	AY00
BD38	VSS_47	VSS_129	AY00	VSS_130	AY00
BD36	VSS_48	VSS_130	AY00	VSS_131	AY00
BD34	VSS_49	VSS_131	AY00	VSS_132	AY00
BD32	VSS_50	VSS_132	AY00	VSS_133	AY00
BD30	VSS_51	VSS_133	AY00	VSS_134	AY00
BD28	VSS_52	VSS_134	AY00	VSS_135	AY00
BD26	VSS_53	VSS_135	AY00	VSS_136	AY00
BD24	VSS_54	VSS_136	AY00	VSS_137	AY00
BD22	VSS_55	VSS_137	AY00	VSS_138	AY00
BD20	VSS_56	VSS_138	AY00	VSS_139	AY00
BD18	VSS_57	VSS_139	AY00	VSS_140	AY00
BD16	VSS_58	VSS_140	AY00	VSS_141	AY00
BD14	VSS_59	VSS_141	AY00	VSS_142	AY00
BD12	VSS_60	VSS_142	AY00	VSS_143	AY00
BD10	VSS_61	VSS_143	AY00	VSS_144	AY00
BD08	VSS_62	VSS_144	AY00	VSS_145	AY00
BD06	VSS_63	VSS_145	AY00	VSS_146	AY00
BD04	VSS_64	VSS_146	AY00	VSS_147	AY00
BD02	VSS_65	VSS_147	AY00	VSS_148	AY00
BD00	VSS_66	VSS_148	AY00	VSS_149	AY00
BD46	VSS_67	VSS_149	AY00	VSS_150	AY00
BD44	VSS_68	VSS_150	AY00	VSS_151	AY00
BD42	VSS_69	VSS_151	AY00	VSS_152	AY00
BD40	VSS_70	VSS_152	AY00	VSS_153	AY00
BD38	VSS_71	VSS_153	AY00	VSS_154	AY00
BD36	VSS_72	VSS_154	AY00	VSS_155	AY00
BD34	VSS_73	VSS_155	AY00	VSS_156	AY00
BD32	VSS_74	VSS_156	AY00	VSS_157	AY00
BD30	VSS_75	VSS_157	AY00	VSS_158	AY00
BD28	VSS_76	VSS_158	AY00	VSS_159	AY00
BD26	VSS_77	VSS_159	AY00	VSS_160	AY00
BD24	VSS_78	VSS_160	AY00	VSS_161	AY00
BD22	VSS_79	VSS_161	AY00	VSS_162	AY00
BD20	VSS_80	VSS_162	AY00	VSS_163	AY00
BD18	VSS_81	VSS_163	AY00	VSS_164	AY00
BD16	VSS_82	VSS_164	AY00	VSS_165	AY00
BD14	VSS_83	VSS_165	AY00	VSS_166	AY00
BD12	VSS_84	VSS_166	AY00	VSS_167	AY00
BD10	VSS_85	VSS_167	AY00	VSS_168	AY00
BD08	VSS_86	VSS_168	AY00	VSS_169	AY00
BD06	VSS_87	VSS_169	AY00	VSS_170	AY00
BD04	VSS_88	VSS_170	AY00	VSS_171	AY00
BD02	VSS_89	VSS_171	AY00	VSS_172	AY00
BD00	VSS_90	VSS_172	AY00	VSS_173	AY00
BD46	VSS_91	VSS_173	AY00	VSS_174	AY00
BD44	VSS_92	VSS_174	AY00	VSS_175	AY00
BD42	VSS_93	VSS_175	AY00	VSS_176	AY00
BD40	VSS_94	VSS_176	AY00	VSS_177	AY00
BD38	VSS_95	VSS_177	AY00	VSS_178	AY00
BD36	VSS_96	VSS_178	AY00	VSS_179	AY00
BD34	VSS_97	VSS_179	AY00	VSS_180	AY00
BD32	VSS_98	VSS_180	AY00	VSS_181	AY00
BD30	VSS_99	VSS_181	AY00	VSS_182	AY00
BD28	VSS_100	VSS_182	AY00	VSS_183	AY00
BD26	VSS_101	VSS_183	AY00	VSS_184	AY00
BD24	VSS_102	VSS_184	AY00	VSS_185	AY00
BD22	VSS_103	VSS_185	AY00	VSS_186	AY00
BD20	VSS_104	VSS_186	AY00	VSS_187	AY00
BD18	VSS_105	VSS_187	AY00	VSS_188	AY00
BD16	VSS_106	VSS_188	AY00	VSS_189	AY00
BD14	VSS_107	VSS_189	AY00	VSS_190	AY00
BD12	VSS_108	VSS_190	AY00	VSS_191	AY00
BD10	VSS_109	VSS_191	AY00	VSS_192	AY00
BD08	VSS_110	VSS_192	AY00	VSS_193	AY00
BD06	VSS_111	VSS_193	AY00	VSS_194	AY00
BD04	VSS_112	VSS_194	AY00	VSS_195	AY00
BD02	VSS_113	VSS_195	AY00	VSS_196	AY00
BD00	VSS_114	VSS_196	AY00	VSS_197	AY00
BD46	VSS_115	VSS_197	AY00	VSS_198	AY00
BD44	VSS_116	VSS_198	AY00	VSS_199	AY00
BD42	VSS_117	VSS_199	AY00	VSS_200	AY00
BD40	VSS_118	VSS_200	AY00	VSS_201	AY00
BD38	VSS_119	VSS_201	AY00	VSS_202	AY00
BD36	VSS_120	VSS_202	AY00	VSS_203	AY00
BD34	VSS_121	VSS_203	AY00	VSS_204	AY00
BD32	VSS_122	VSS_204	AY00	VSS_205	AY00
BD30	VSS_123	VSS_205	AY00	VSS_206	AY00
BD28	VSS_124	VSS_206	AY00	VSS_207	AY00
BD26	VSS_125	VSS_207	AY00	VSS_208	AY00
BD24	VSS_126	VSS_208	AY00	VSS_209	AY00
BD22	VSS_127	VSS_209	AY00	VSS_210	AY00
BD20	VSS_128	VSS_210	AY00	VSS_211	AY00
BD18	VSS_129	VSS_211	AY00	VSS_212	AY00
BD16	VSS_130	VSS_212	AY00	VSS_213	AY00
BD14	VSS_131	VSS_213	AY00	VSS_214	AY00
BD12	VSS_132	VSS_214	AY00	VSS_215	AY00
BD10	VSS_133	VSS_215	AY00	VSS_216	AY00
BD08	VSS_134	VSS_216	AY00	VSS_217	AY00
BD06	VSS_135	VSS_217	AY00	VSS_218	AY00
BD04	VSS_136	VSS_218	AY00	VSS_219	AY00
BD02	VSS_137	VSS_219	AY00	VSS_220	AY00
BD00	VSS_138	VSS_220	AY00	VSS_221	AY00
BD46	VSS_139	VSS_221	AY00	VSS_222	AY00
BD44	VSS_140	VSS_222	AY00	VSS_223	AY00
BD42	VSS_141	VSS_223	AY00	VSS_224	AY00
BD40	VSS_142	VSS_224	AY00	VSS_225	AY00
BD38	VSS_143	VSS_225	AY00	VSS_226	AY00
BD36	VSS_144	VSS_226	AY00	VSS_227	AY00
BD34	VSS_145	VSS_227	AY00	VSS_228	AY00
BD32	VSS_146	VSS_228	AY00	VSS_229	AY00
BD30	VSS_147	VSS_229	AY00	VSS_230	AY00
BD28	VSS_148	VSS_230	AY00	VSS_231	AY00
BD26	VSS_149	VSS_231	AY00	VSS_232	AY00
BD24	VSS_150	VSS_232	AY00	VSS_233	AY00
BD22	VSS_151	VSS_233	AY00	VSS_234	AY00
BD20	VSS_152	VSS_234	AY00	VSS_235	AY00
BD18	VSS_153	VSS_235	AY00	VSS_236	AY00
BD16	VSS_154	VSS_236	AY00	VSS_237	AY00
BD14	VSS_155	VSS_237	AY00	VSS_238	AY00
BD12	VSS_156	VSS_238	AY00	VSS_239	AY00
BD10	VSS_157	VSS_239	AY00	VSS_240	AY00
BD08	VSS_158	VSS_240	AY00	VSS_241	AY00
BD06	VSS_159	VSS_241	AY00	VSS_242	AY00
BD04	VSS_160	VSS_242	AY00	VSS_243	AY00
BD02	VSS_161	VSS_243	AY00	VSS_244	AY00
BD00	VSS_162	VSS_244	AY00	VSS_245	AY00
BD46	VSS_163	VSS_245	AY00	VSS_246	AY00
BD44	VSS_164	VSS_246	AY00	VSS_247	AY00
BD42	VSS_165	VSS_247	AY00	VSS_248	AY00
BD40	VSS_166	VSS_248	AY00	VSS_249	AY00
BD38	VSS_167	VSS_249	AY00	VSS_250	AY00
BD36	VSS_168	VSS_250	AY00	VSS_251	AY00
BD34	VSS_169	VSS_251	AY00	VSS_252	AY00
BD32	VSS_170	VSS_252	AY00	VSS_253	AY00
BD30	VSS_171	VSS_253	AY00	VSS_254	AY00
BD28	VSS_172	VSS_254	AY00	VSS_255	AY00
BD26	VSS_173	VSS_255	AY00	VSS_256	AY00
BD24	VSS_174	VSS_256	AY00	VSS_257	AY00
BD22	VSS_175	VSS_257	AY00	VSS_258	AY00
BD20	VSS_176	VSS_258	AY00	VSS_259	AY00
BD18	VSS_177	VSS_259	AY00	VSS_260	AY00
BD16	VSS_178	VSS_260	AY00	VSS_261	AY00
BD14	VSS_179	VSS_261	AY00	VSS_262	AY00
BD12	VSS_180	VSS_262	AY00	VSS_263	AY00
BD10	VSS_181	VSS_263	AY00	VSS_264	AY00
BD08	VSS_182	VSS_264	AY00	VSS_265	AY00
BD06	VSS_183	VSS_265	AY00	VSS_266	AY00
BD04	VSS_184	VSS_266	AY00	VSS_267	AY00
BD02	VSS_185	VSS_267	AY00	VSS_268	AY00
BD00	VSS_186	VSS_268	AY00	VSS_269	AY00
BD46	VSS_187	VSS_269	AY00	VSS_270	AY00
BD44	VSS_188	VSS_270	AY00	VSS_271	AY00
BD42	VSS_189	VSS_271	AY00	VSS_272	AY00
BD40	VSS_190	VSS_272	AY00	VSS_273	AY00
BD38	VSS_191	VSS_273	AY00	VSS_274	AY00
BD36	VSS_192	VSS_274	AY00	VSS_275	AY00
BD34	VSS_193	VSS_275	AY00	VSS_276	AY00
BD32	VSS_194	VSS_276	AY00	VSS_277	AY00
BD30	VSS_195	VSS_277	AY00	VSS_278	AY00
BD28	VSS_196	VSS_278	AY00	VSS_279	AY00
BD26	VSS_197	VSS_279	AY00	VSS_280	AY00
BD24	VSS_198	VSS_280	AY00	VSS_281	AY00
BD22	VSS_199	VSS_281	AY00	VSS_282	AY00
BD20	VSS_200	VSS_282	AY00	VSS_283	AY00
BD18	VSS_201	VSS_283	AY00	VSS_284	AY00
BD16	VSS_202	VSS_284	AY00	VSS_285	AY00
BD14	VSS_203	VSS_285	AY00	VSS_286	AY00
BD12	VSS_204	VSS_286	AY00	VSS_287	AY00
BD10	VSS_205	VSS_287	AY00	VSS_288	AY00
BD08	VSS_206	VSS_288	AY00	VSS_289	AY00
BD06	VSS_207	VSS_289	AY00	VSS_290	AY00
BD04	VSS_208	VSS_290	AY00	VSS_291	AY00
BD02	VSS_209	VSS_291	AY00	VSS_292	AY00
BD00	VSS_210	VSS_292	AY00	VSS_293	AY00
BD46	VSS_211	VSS_293	AY00	VSS_294	AY00
BD44	VSS_212	VSS_294	AY00	VSS_295	AY00
BD42	VSS_213	VSS_295	AY00	VSS_296	AY00
BD40	VSS_214	VSS_296	AY00	VSS	

# SO-DIMM(DDR)



Close to DIMM



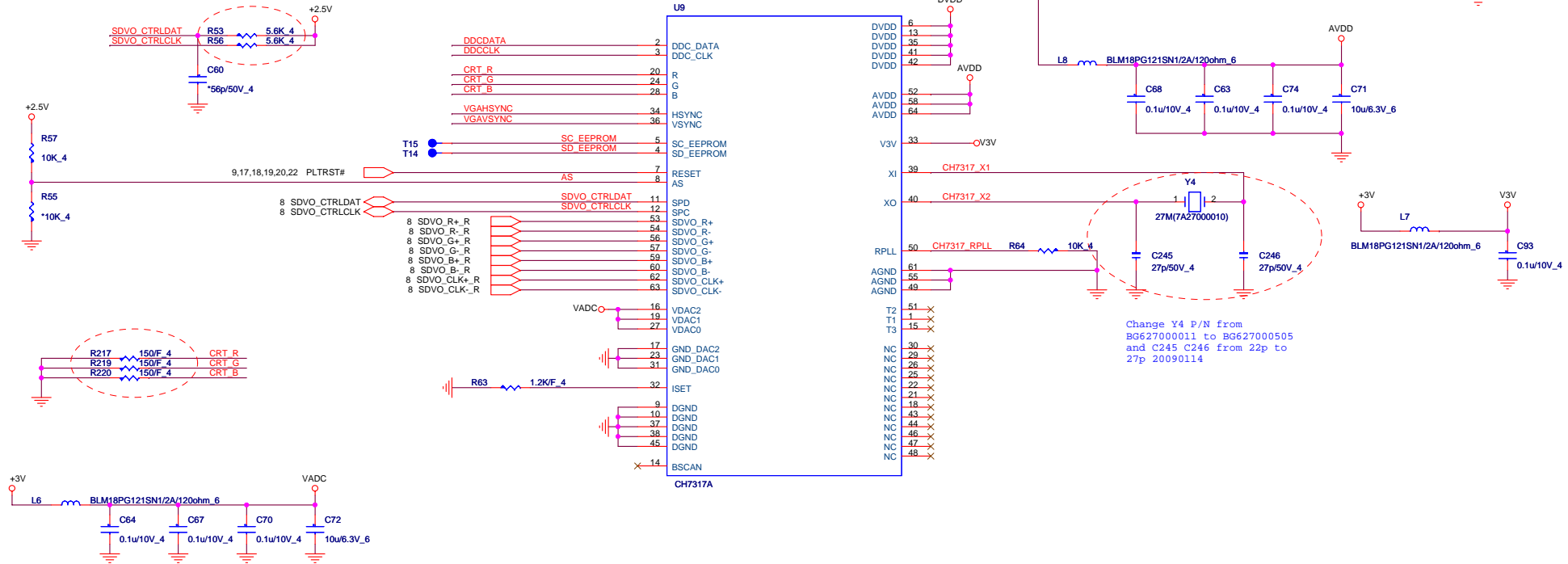


**Quanta Computer Inc.**  
**PROJECT : ZA3**

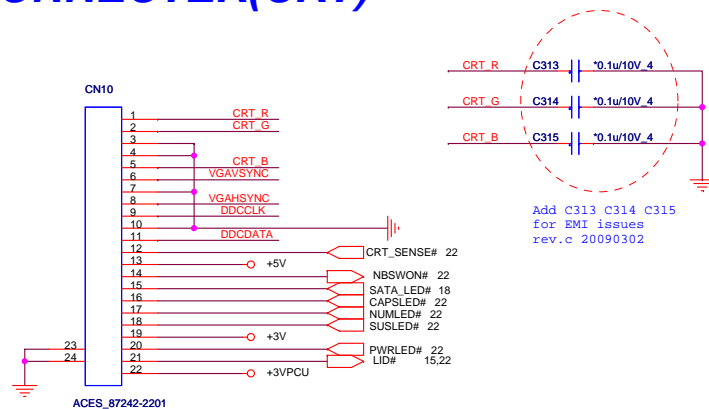
Size	Document Number	Rev
	<b>DDR2 SO-DIMM(200P)</b>	1A
Date:	Sunday, March 08, 2009	Sheet 13 of 34

***SDVO To CRT(CRT)***

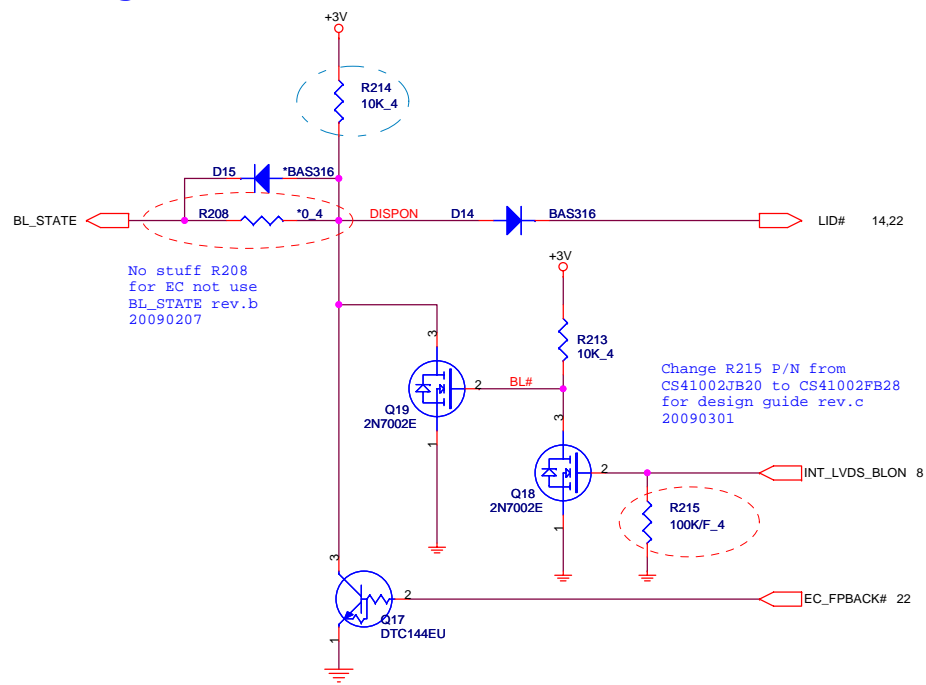
For vender FAE check, Change R53  
R56 from 3.9K to 5.6K 20081205



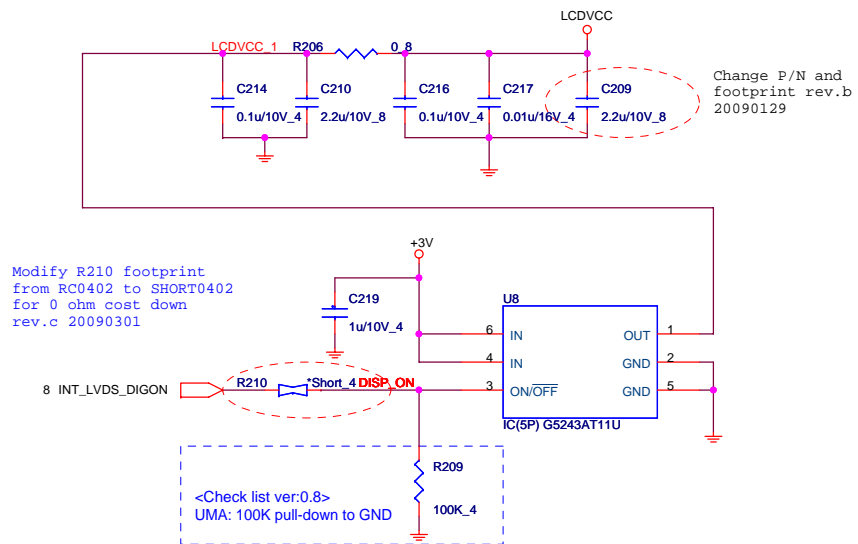
## ***CRT DB CONNECTER(CRT)***



## Backlight Control(LDS)

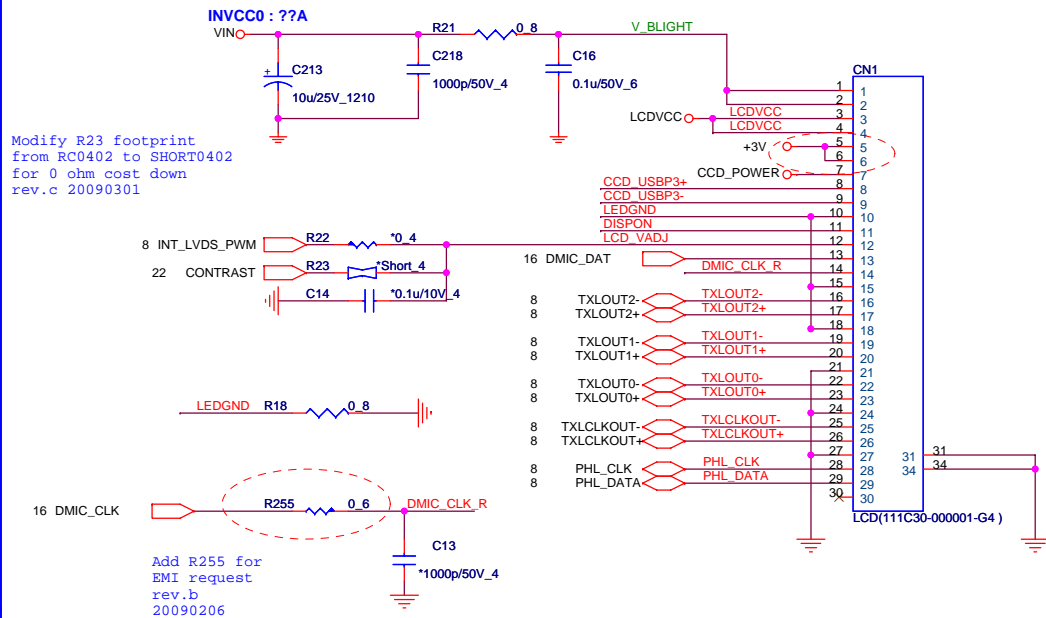


## LED Panel POWER SWITCH(LDS)

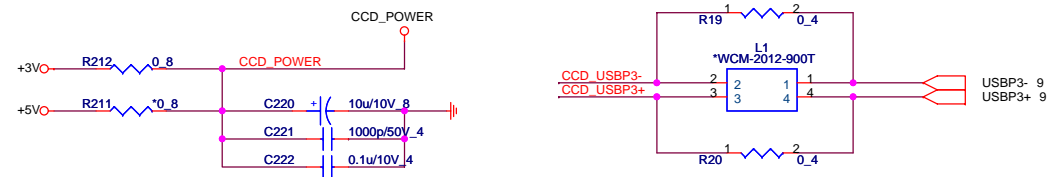


## LED Panel(LDS)

***V\_BLIGHT : ?V ?A***



## Camera(CCD)



Size	Document Number <b>LED PANEL/CCD MODULE</b>	Rev 1A
Date:	Sunday, March 08, 2009	Sheet 15 of 34



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## MUTE(AMP)



## HDA Power(ADO)



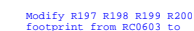
### System MIC\_Pink ESD(EMC)



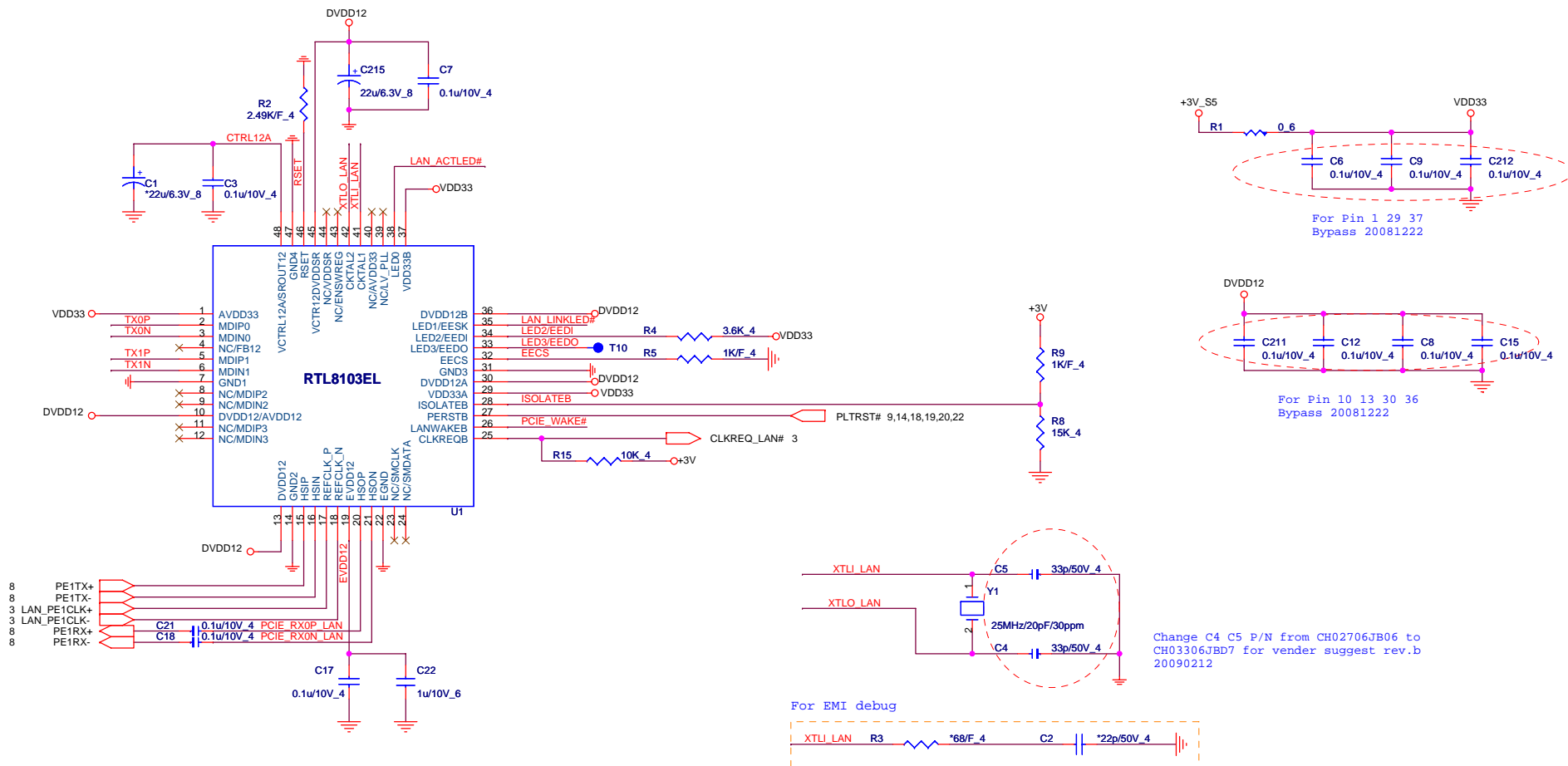
```

y R197 R198 R199 R200
print from RC0603 to

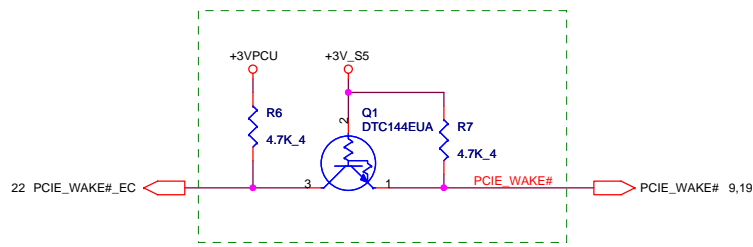
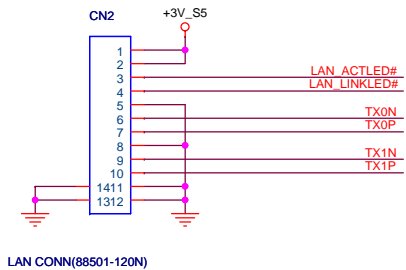
```



# LAN RTL8103EL (LAN)

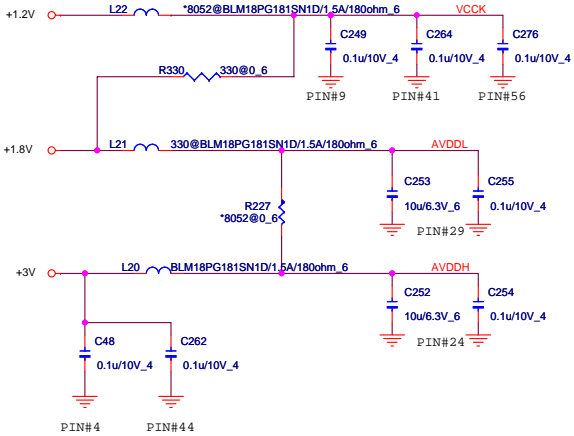


## LAN D/B CONNECTER(LAN)

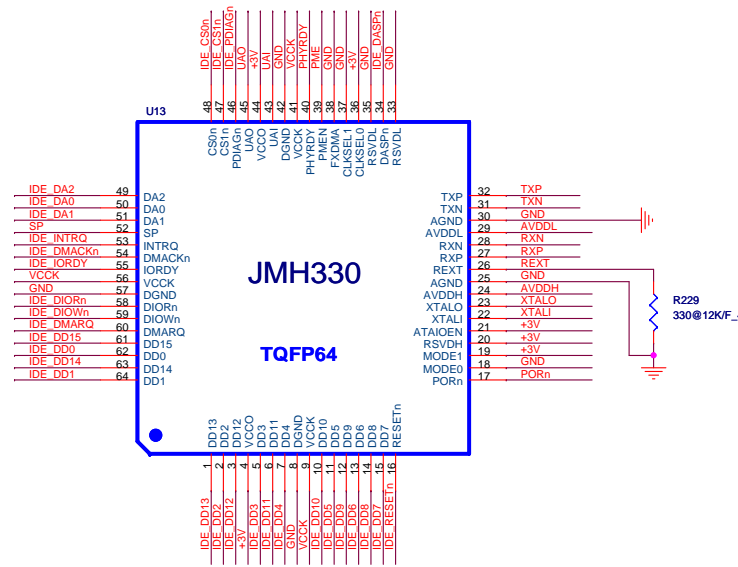
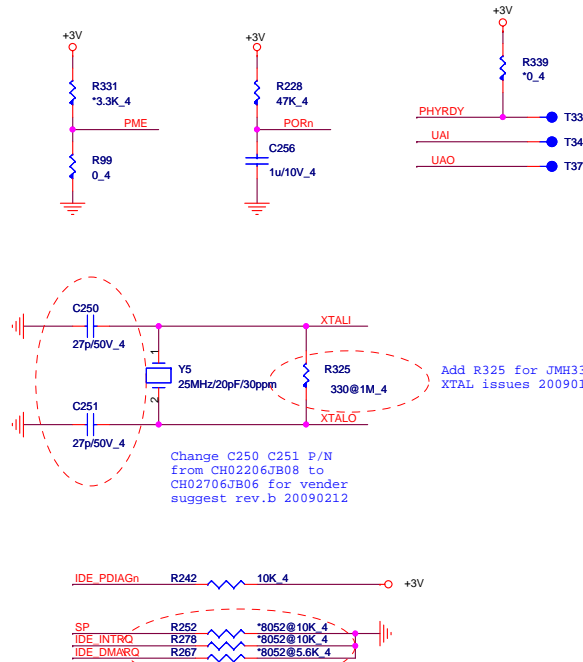


# PATA TO SATA BRIDGE(HDD)

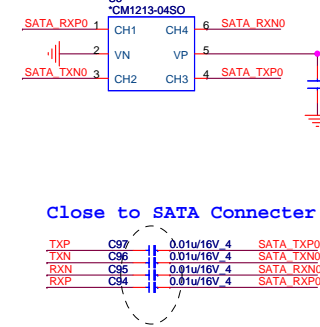
Bypass CAP must place close to power pins



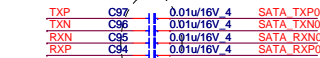
PME



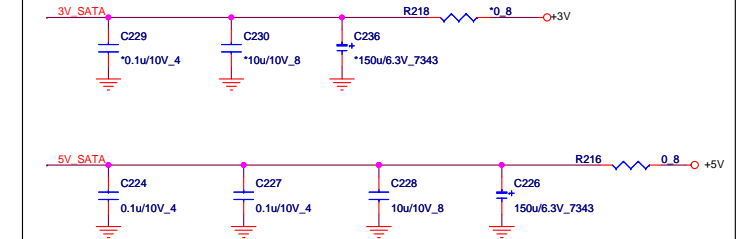
## SATA ESD(EMC)



Close to SATA Connector



## SATA POWER(HDD)



Del RN20 and add RN21  
RN22 20090113

	JM330 (AJ003300H00)	88SA8052 (AJ080520H00)
Stuff	L21 R330 R325	L22 R227
No Stuff	L22 R227	L21 R330 R325
Change	R229 = 12K	R229 = 6.04K

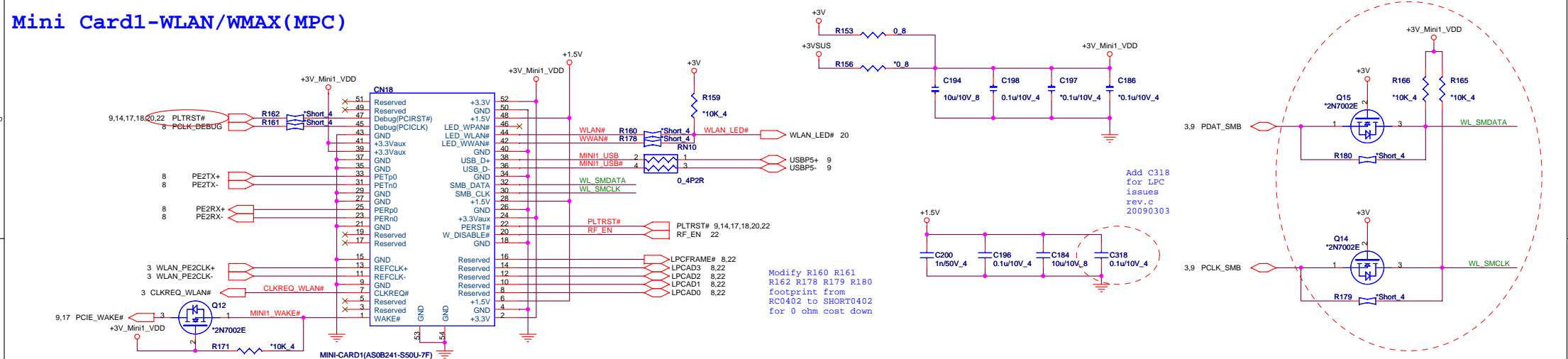
For JM330 FAE Check : Can change RN20 R269 R270 R272 R274 from 82ohm to 0ohm, R268 R271 R273 from 22ohm to 0ohm, RN12 RN13 RN14 RN15 RN16 RN17 RN18 RN19 R233 from 33ohm to 0ohm 20081223

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PROJECT : ZA3

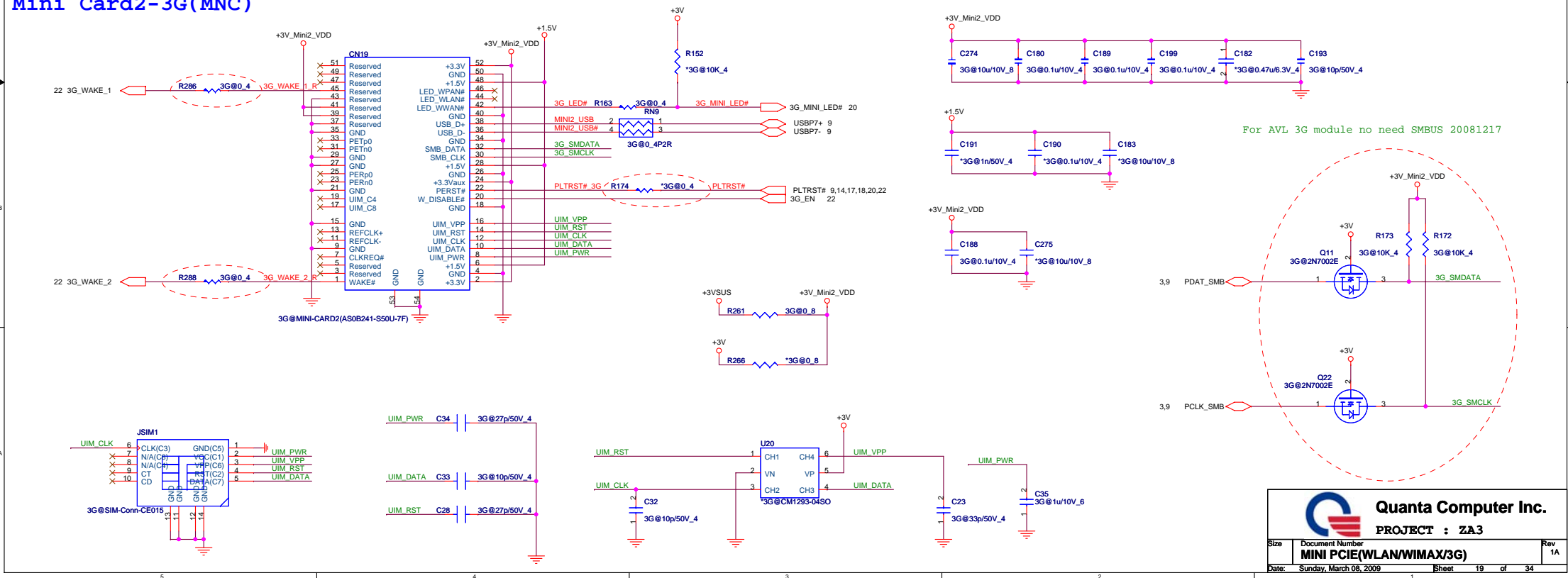
Size: Document Number: **PATA TO SATA BRIDGE(88SA8052)** Rev 1A

Date: Sunday, March 08, 2009 Sheet 18 of 34

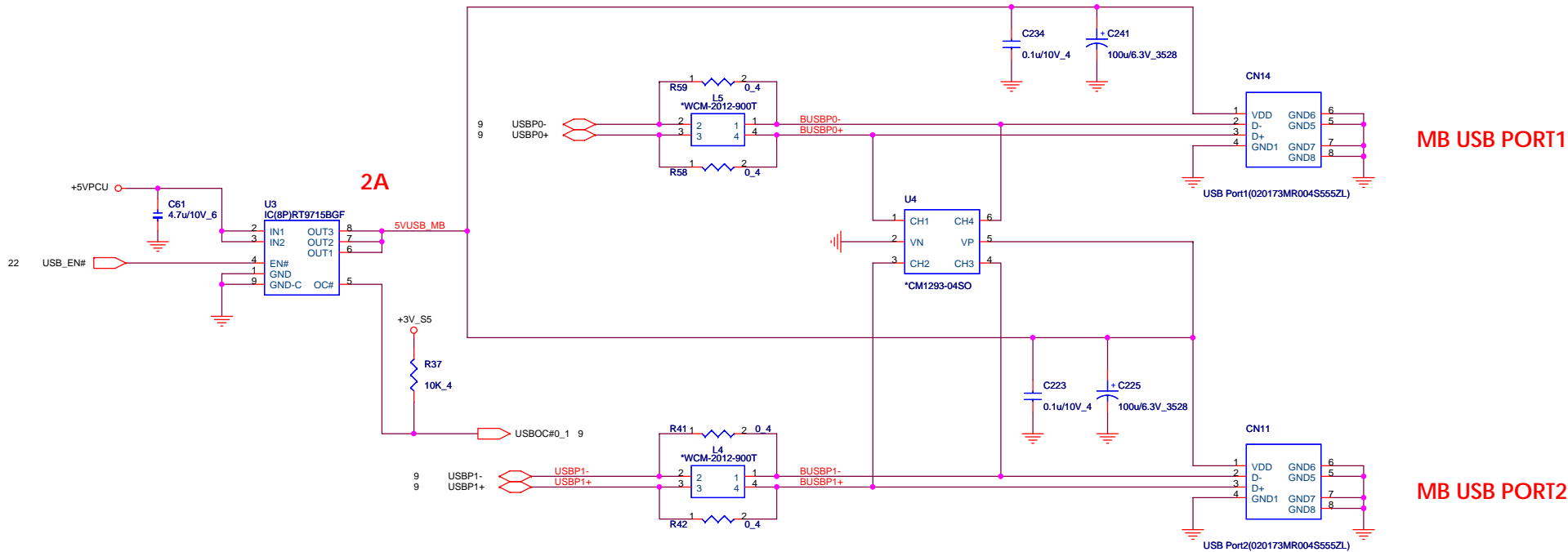
## Mini Card1-WLAN/WMAX(MPC)



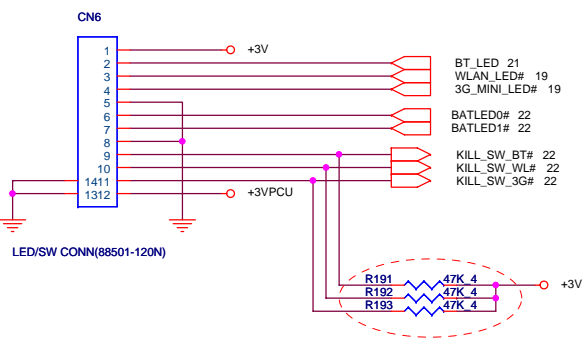
## Mini Card2-3G(MNC)



# MB USB PORTS(USB)

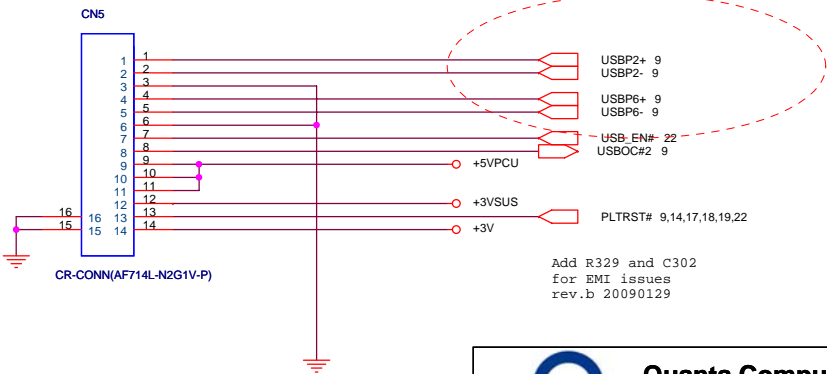



# LED DB CONNECTER(UIF)



EC GPIO	Button
KILL_SW_WL#(GPIO57 PIN33)	WLAN Switch
KILL_SW_3G#(GPIO60 PIN34)	3G Switch
KILL_SW_BT#(GPIO12 PIN13)	BT Switch

# Card Reader/USB DB CONNECTER(MMC)



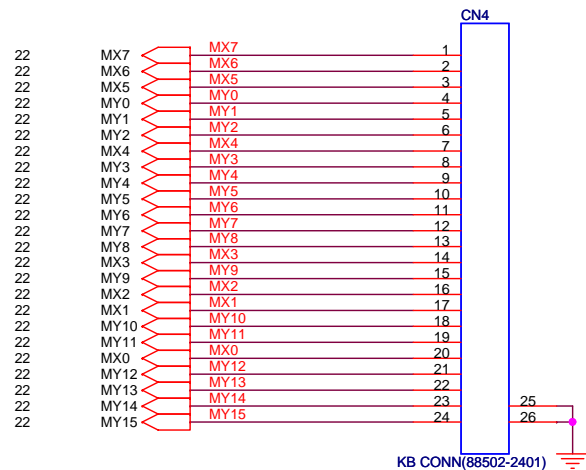


Quanta Computer Inc.

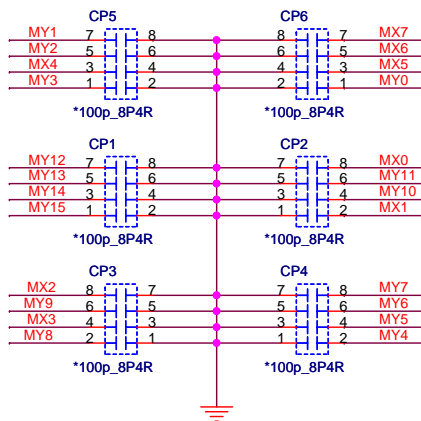
PROJECT : ZA3

Size	Document Number	Rev
	USB/SD_LED AND CR_USB DB	1A
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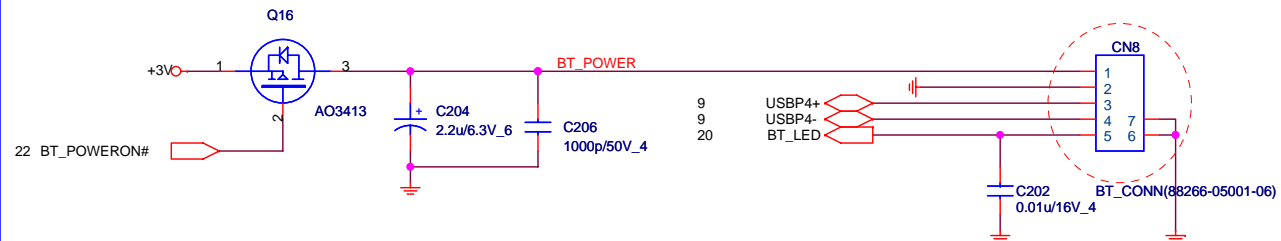
# Keyboard (KBC)



For EMI Reserve Caps for debug

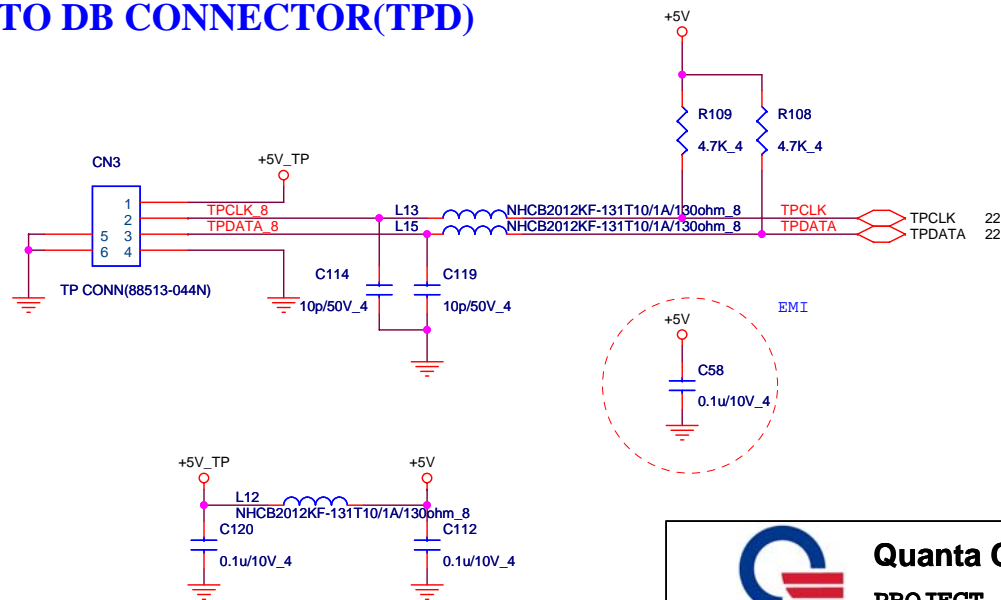


# BT CONNECTER (BTM)



Modify CN8 footprint and pin define rev.c 20090301

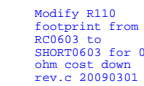
# TO DB CONNECTOR(TPD)



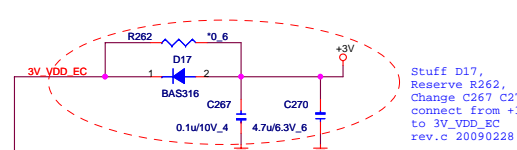
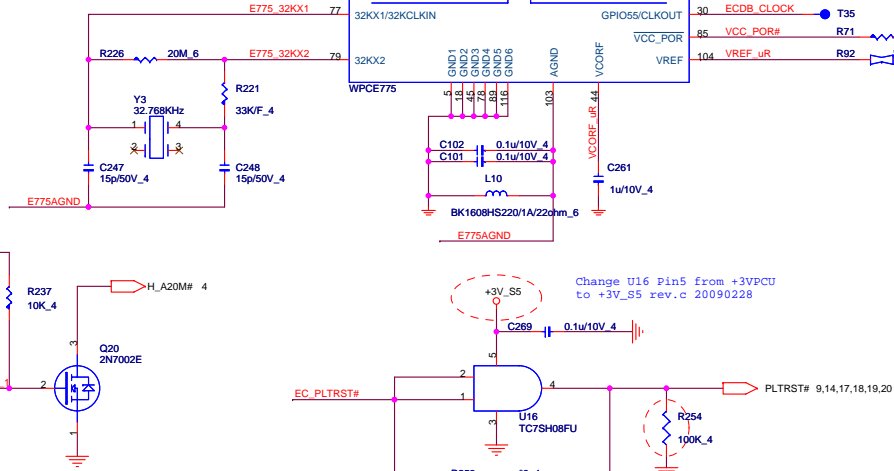
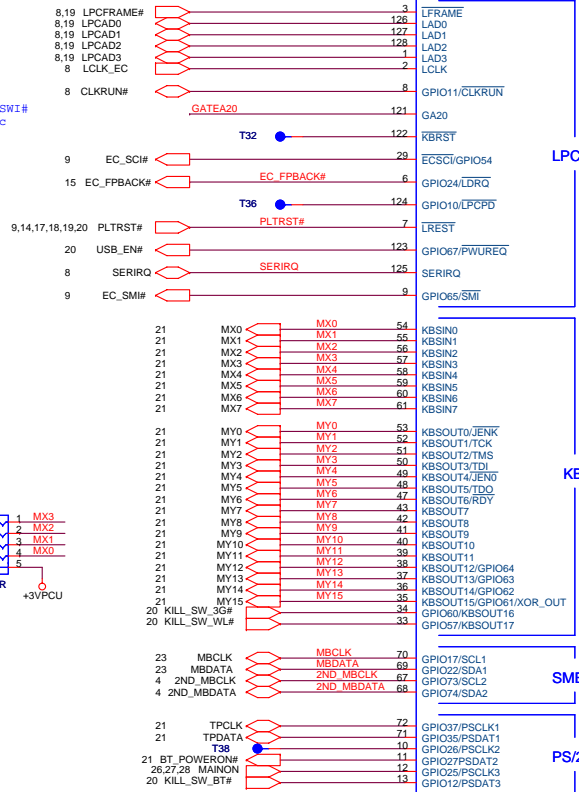
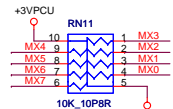
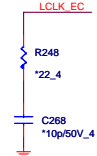
Quanta Computer Inc.  
PROJECT : ZA3

Size	Document Number	Rev
	KB/BT/TP	1A
Date:	Sunday, March 08, 2009	Sheet 21 of 34

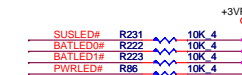
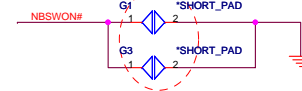
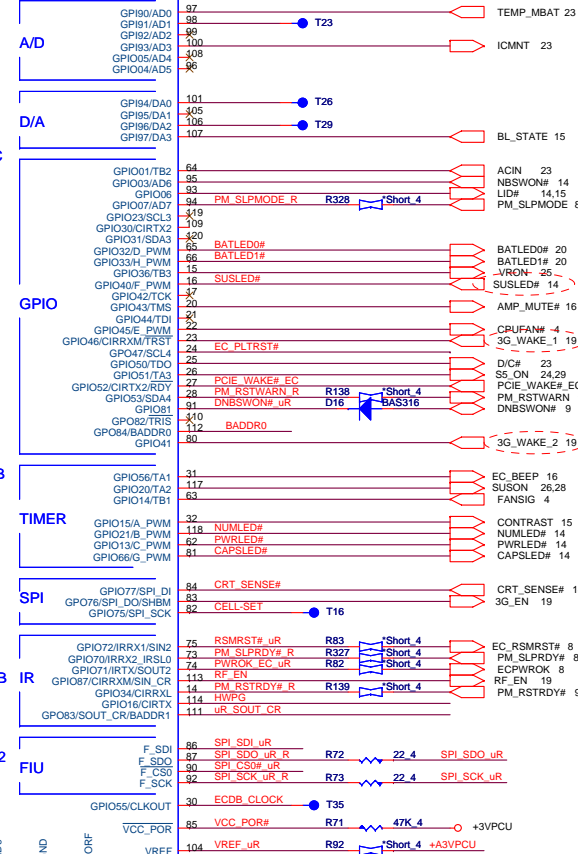
## EC(KBC)



Del D6 for SWI#  
issues rev.c  
20090303



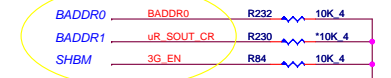
Stuff D17,  
Reserve R262,  
Change C267 C27  
connect from +  
to 3V\_VDD\_EC  
rev.c 20090228



## I/O ADDRESS SETTING

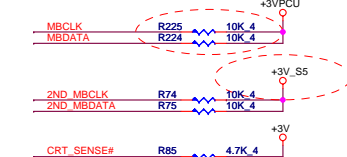
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

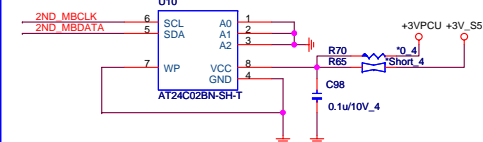


1/13 Confirm by vendor mail :  
Disabled ('1') if using FWH device on LPC.  
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

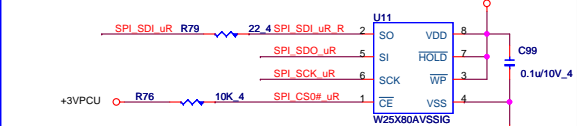
## SM BUS PU



## ACER ID

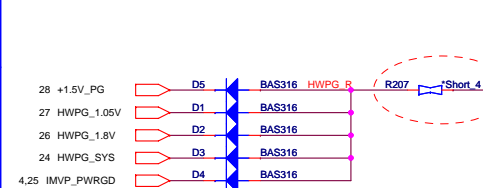


## SPI FLASH



1/13 Confirm by vendor mail :  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

**HWPG**



## INTERNAL KEYBOARD STRIP SET

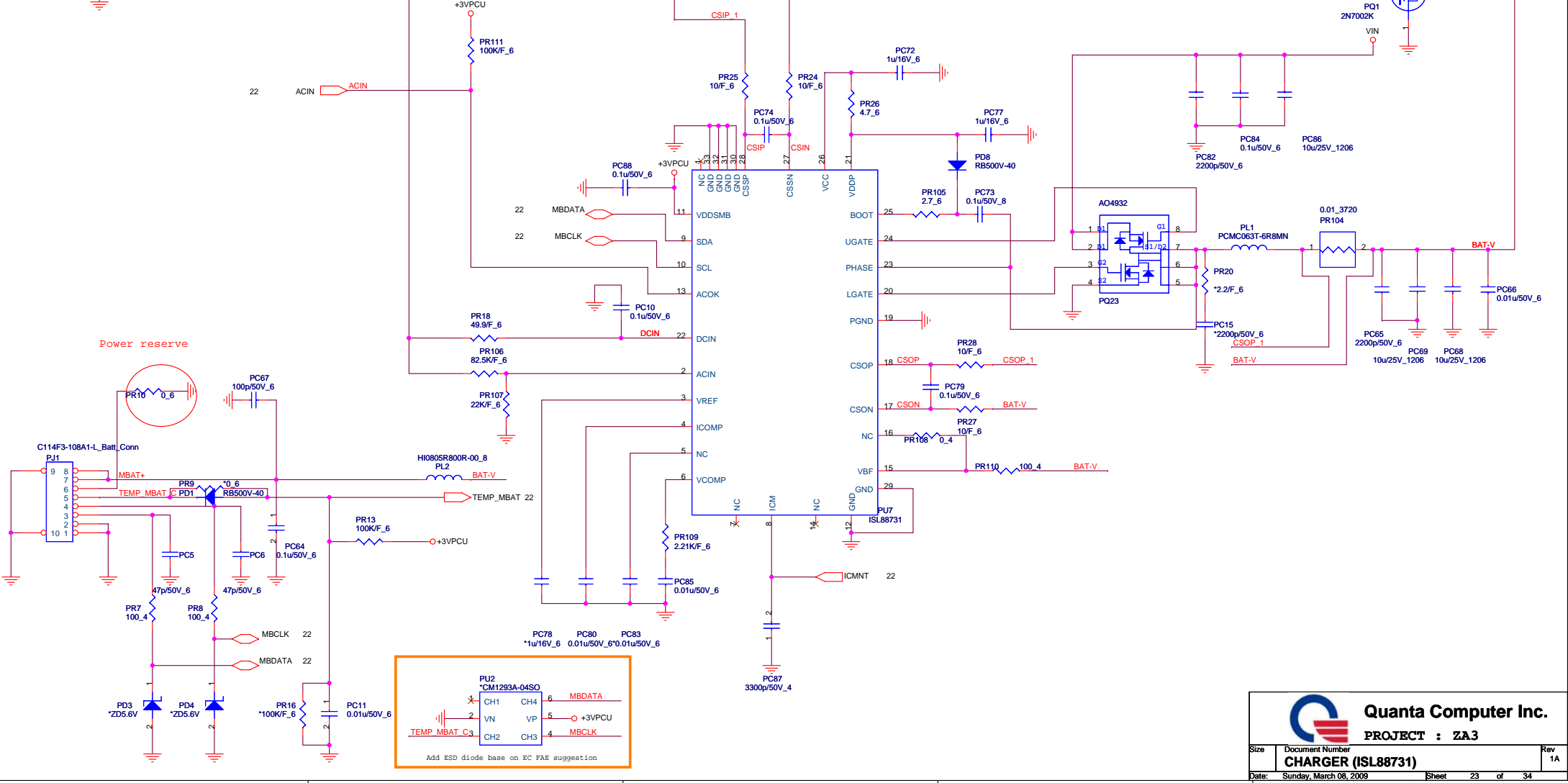
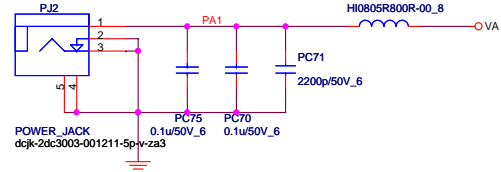


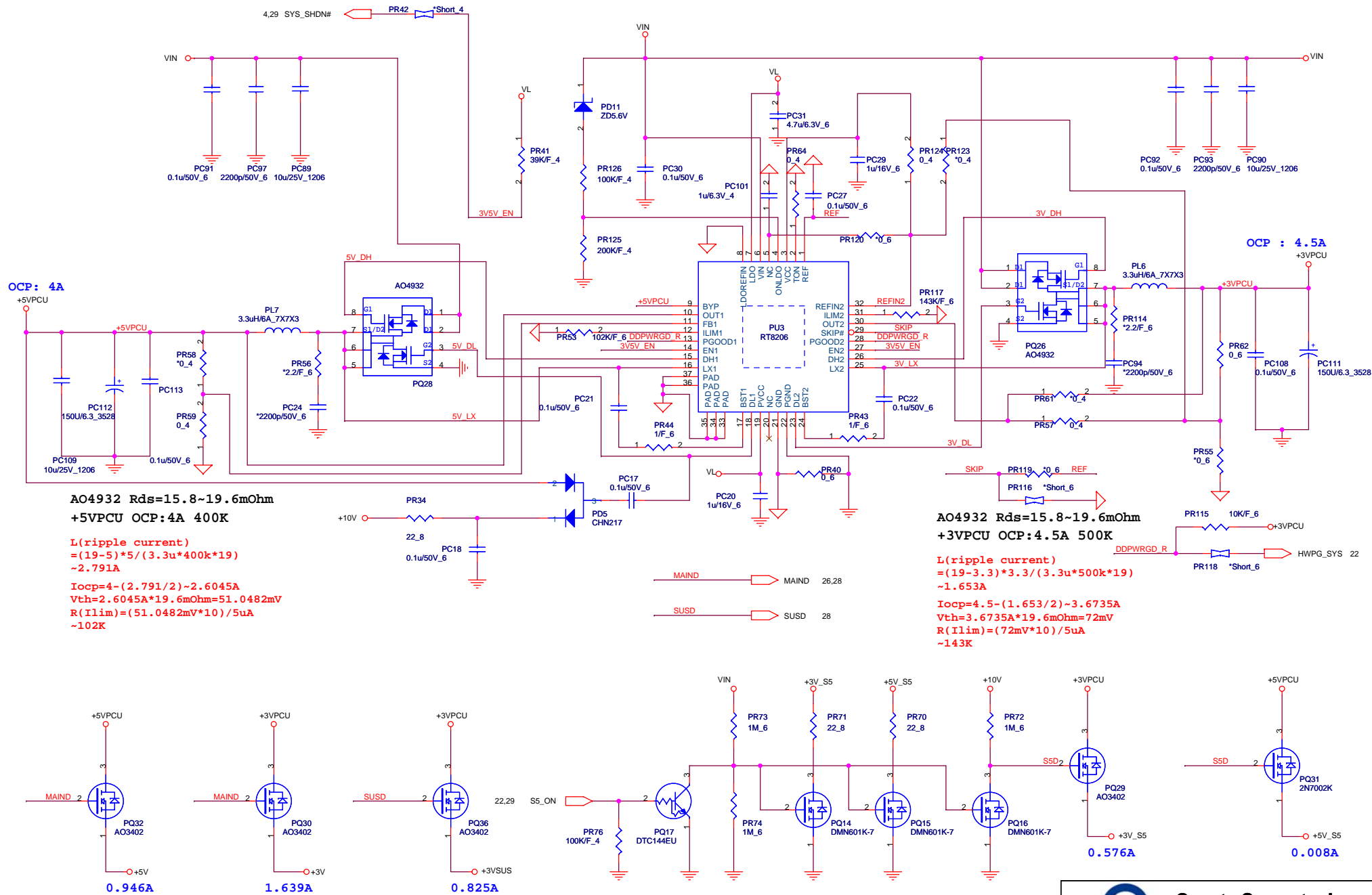
**Quanta Computer Inc.**

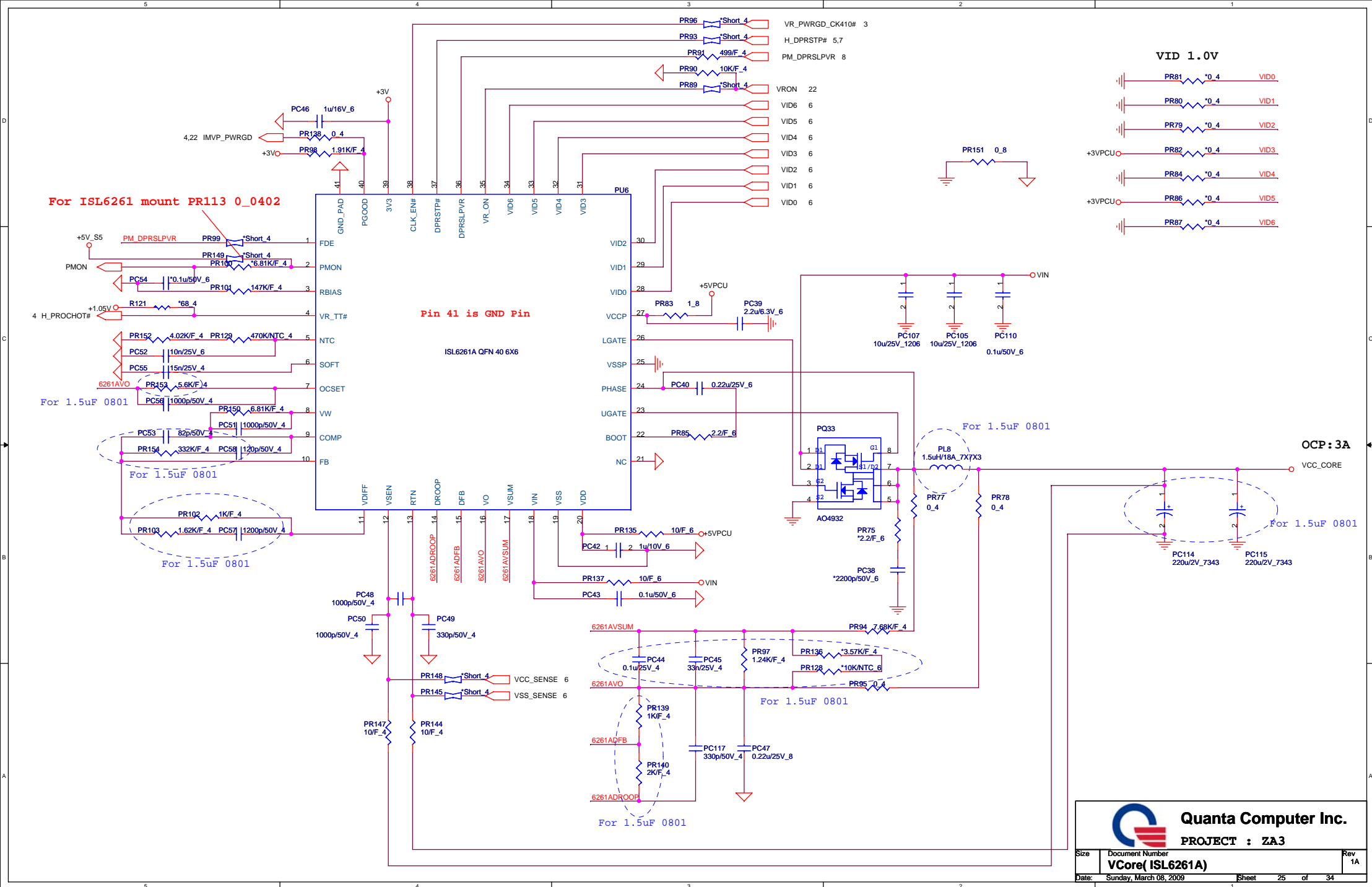
Size	Document Number <b>WPCE775C/FLASH</b>	Rev 1A
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65W Yellow DFPJ05MR007

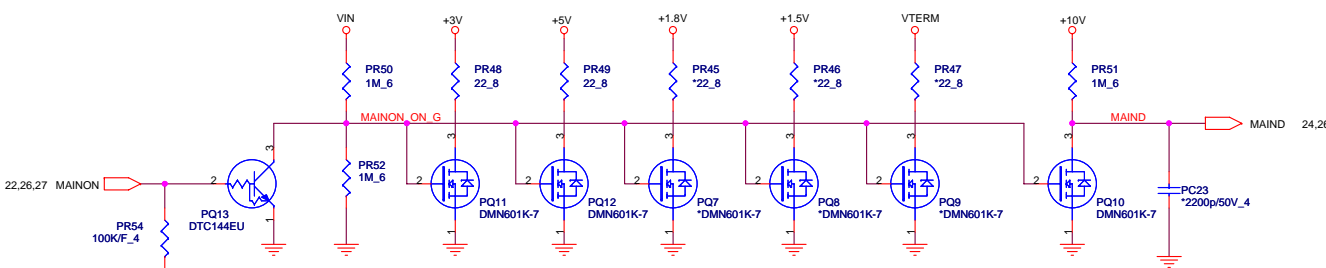
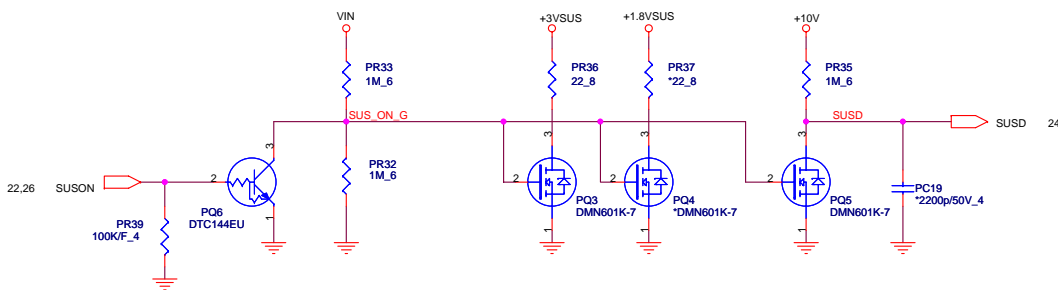
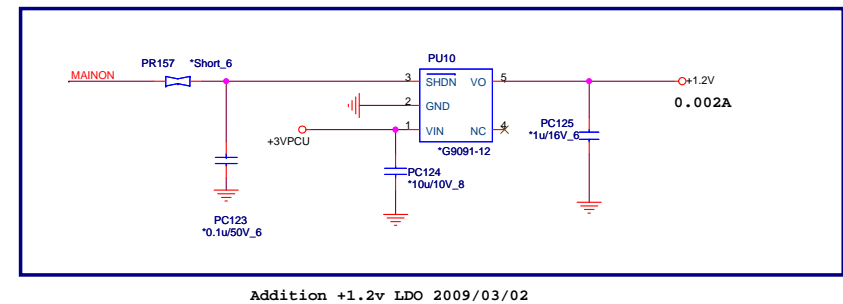
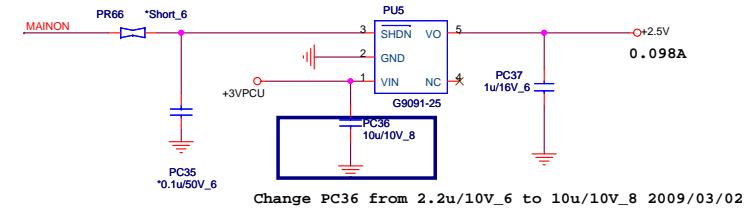
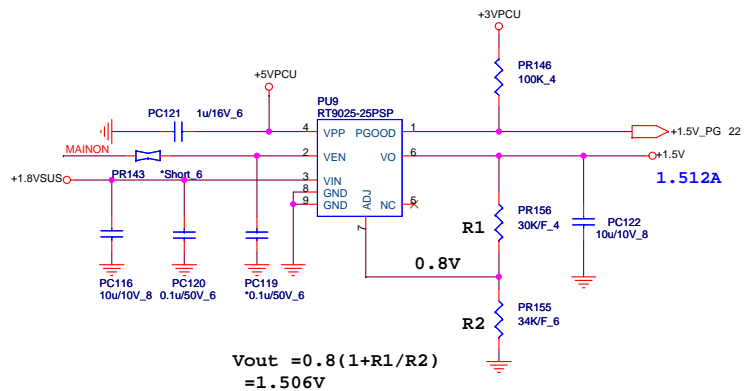


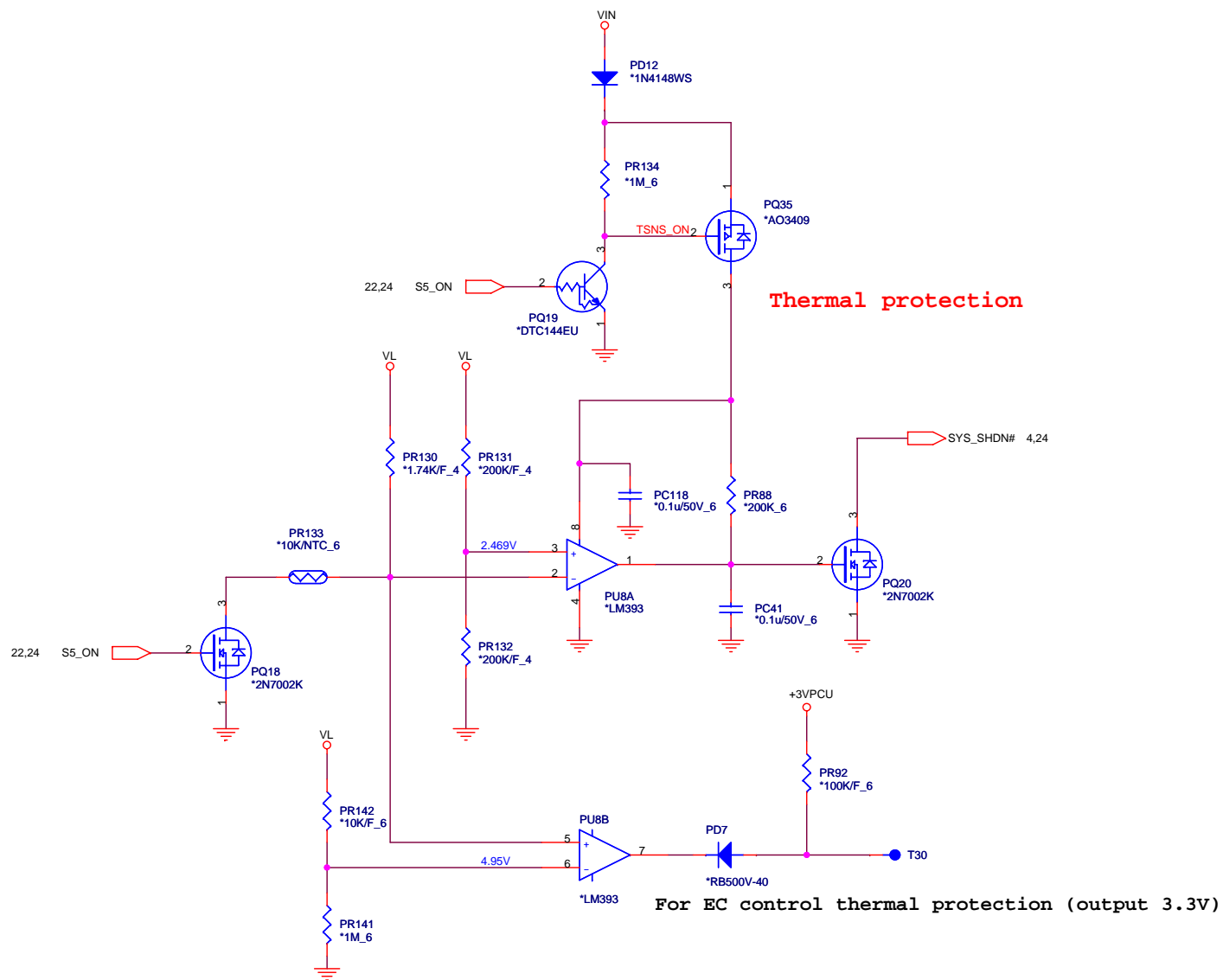






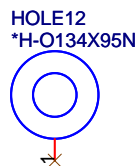
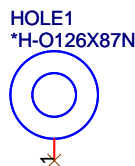
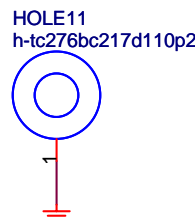
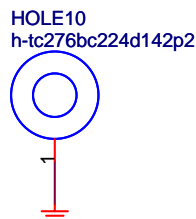
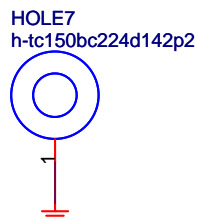
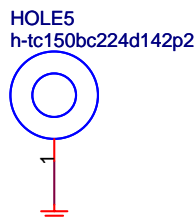
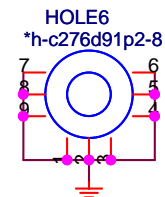
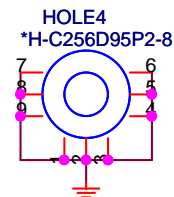
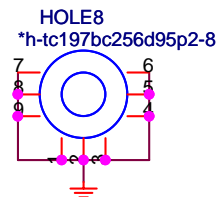
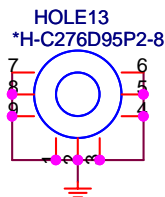
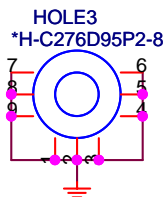
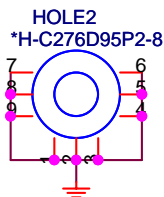




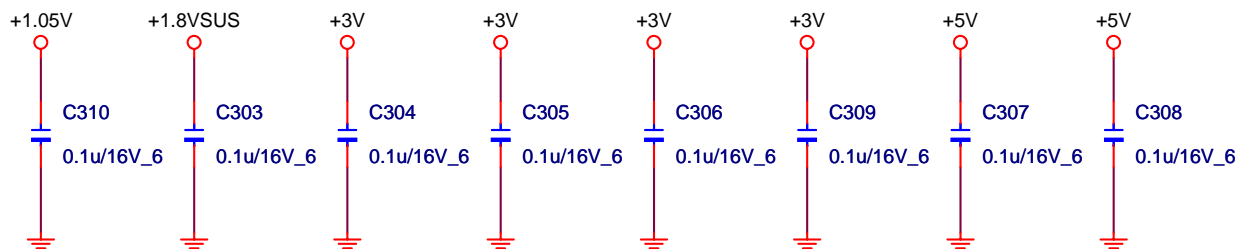




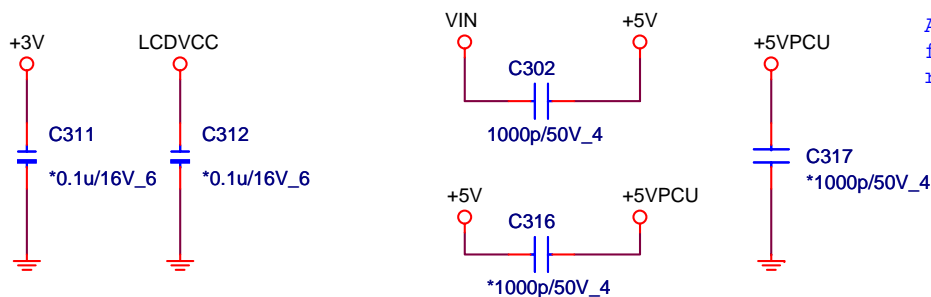
# HOLES



# EMI



Add C303 C304 C305 C306 C307  
C308 for EMI request rev.b  
20090206 Add C309 C310 for  
EMI request rev.b 20090207



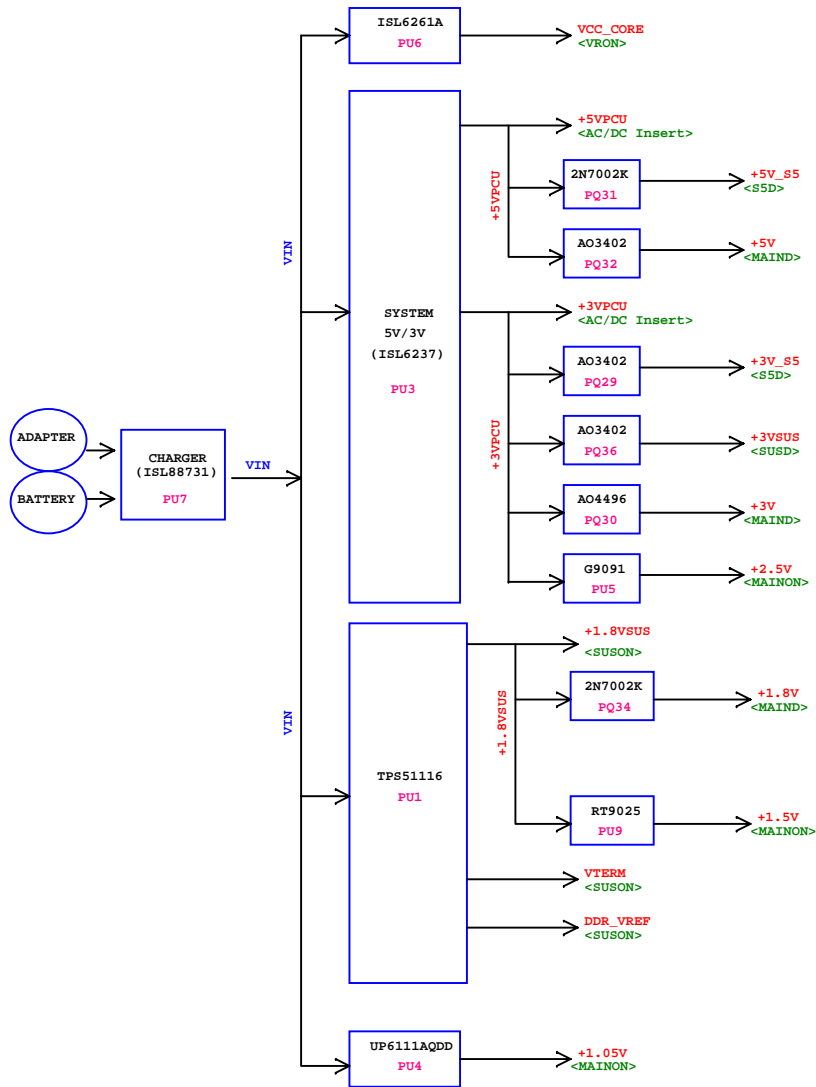
Add C302 C316 C317  
for EMI issues  
rev.c 20090303



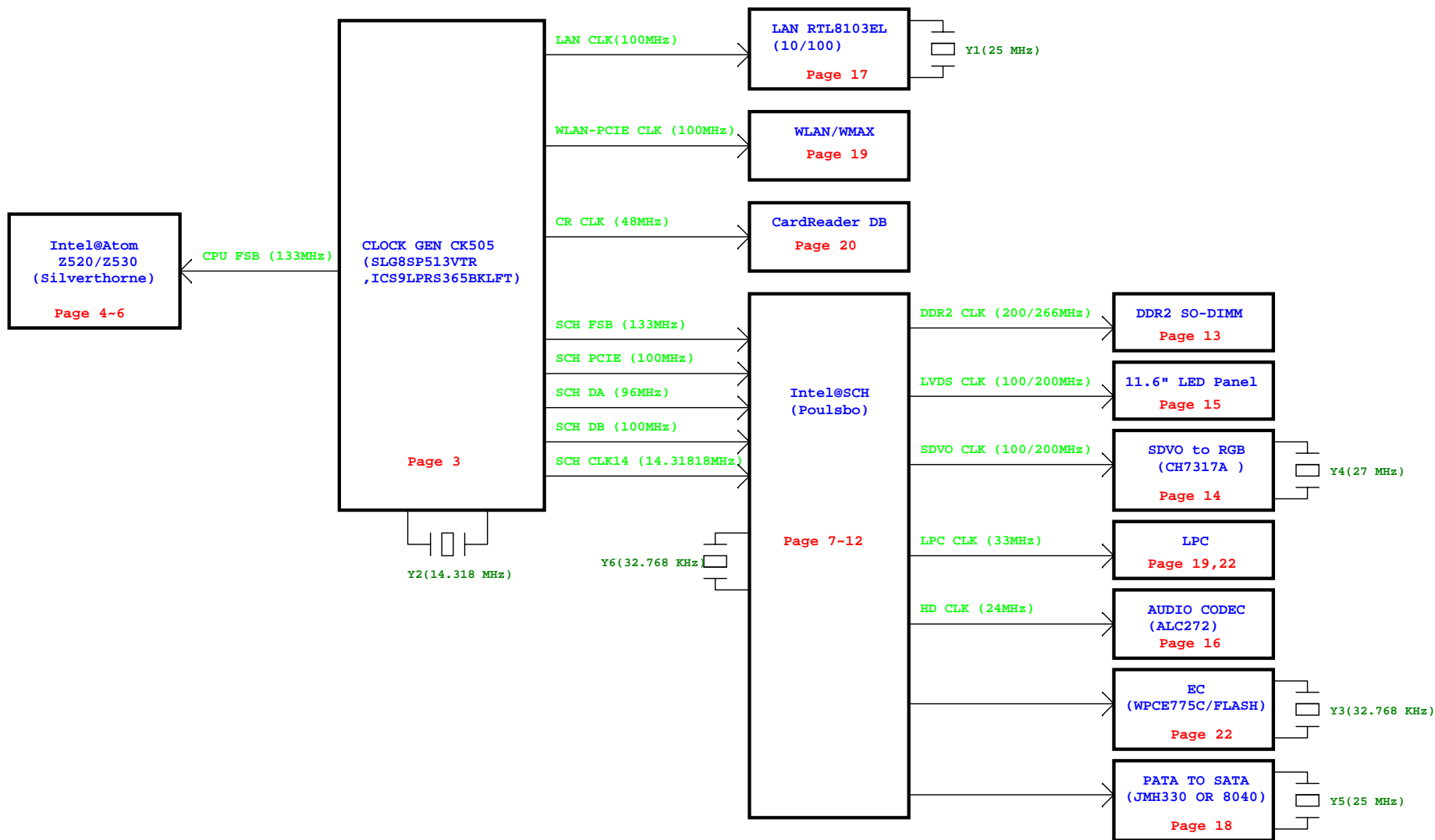
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Size	Document Number	Rev
	<b>HOLE</b>	1A
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POWER	Distribution
VCC_CORE	CPU
+5VPCU	RTC, USB Connector
+5V_S5	SCH Power
+5V	CPU C6-Power Circuit, SCH Power, CRT, LCD, CAMERA ,Audio Code, INT SPK AMP, SATA HDD,Touch Pad
+3VPCU	RTC, LED Power, HALL SENSOR, EC, ID , SPI Flash ,
+3V_S5	SCH USB Power, LAN, ID
+3VSUS	WLAN/WMAX, 3G
+3V	CLK_GEN Power, Thermal Sensor Power, CPU Pull Up Power, SCH Pull Up Power, SCH Power, DDRII Power, SDVO to CRT Power, LCD Power, INT SPK AMP, PATA To SATA Bridge, SATA, WLAN/WMAX, 3G, Card Reader, BT, EC,
+2.5V	SDVO to CRT
+1.8VSUS	SCH Power, DDRII SO-DIMM
+1.8V	PATA To SATA Bridge
+1.5V	CPU, SCH, WLAN/WMAX, 3G
VTERM	DDRII SO-DIMM
DDR_VREF	DDRII SO-DIMM
+1.05V	CLK_GEN, CPU, SCH,



Model	REV	DATE	CHANGE LIST	NOTE
ZA3	A1A	20090107	PAGE16 : Reverse C301 R322 U19 R323 R324 for SPK AMP Power	ECN Release
		20090112	PAGE23 : Change PJ1 P/N and Footprint	
		20090113	PAGE18 : Del RN20 and add RN21 RN22 for HDD issues	
			PAGE18 : Add R325 for JMH330 XTAL issues	
			PAGE21 : Change CN4 P/N from DFFC24FR023 to DFFC24FR017	
			PAGE21 : Change CN4 footprint	
			PAGE20 : Change CN5 P/N from DFFC14FR080 to DFFC14FR047	
			PAGE20 : Change CN6 P/N from DFFC12FR293 to DFFC12FR019	
			PAGE17 : Change CN2 P/N from DFFC12FR293 to DFFC12FR019	
			PAGE20 : Change CN5 footprint from BL121-14R-TAND-14P-L-BU1 to af714l-n2g1x-14p-l	
			PAGE19 : Change ESD1 value to U20	
			PAGE16 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE16 : Change CN7 footprint from 88460-0401-4p-l to 88266-040xx-xxx-4p-l	
			PAGE4 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE4 : Change CN7 footprint from 88460-0401-4p-l to 88266-040xx-xxx-4p-r	
			PAGE21 : Change CN8 P/N from DFHS05FS000 to DFHD05MRD98	
			PAGE21 : Change CN8 footprint from 88460-0501-5P-L to 88266-0500x-5p-l	
			PAGE6 : Del Q10 R138R139 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Change R168 P/N from CS41002FB28 to CS31002JB28 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Add R326 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Change R148 P/N from CS41002FB28 to CS33302JB16 for modify +1.05V_C6_OFF circuit	
			PAGE6 : Add Q26 for modify +1.05V_C6_OFF circuit	
		20090114	PAGE22 : Add R138 R139 R327 R328 for power sequence debug	
			PAGE5 : Add T54 T56 T57 T58 for power sequence debug	
			PAGE4 : Add T55 T59 for power sequence debug	
			PAGE14 : Change Y4 footprint from XTAL-3_2X2_5-2_3X1_9 to xtl-5x3_2-3_7 for cost down issues	
			PAGE14 : Change Y4 P/N from BG627000011 to BG627000505 for cost down issues	
			PAGE17 : Change U1 P/N from AL08103EB00 to AL008103B00	
		20090115	PAGE15 : Change CN1 footprint from MSC-RB30-5-FG-30P-L to msc-rb30-5-fg-30p-l-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change JSIM1 footprint from SIM-CE01X-3-14P to sim-ce01x-3-14p-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change CN18 footprint from micpie-88956-5204-52p-ruv-v to micpie-88956-5204-52p-ruv-v-za3 for ZA3 A-test SMT issues	
			PAGE19 : Change CN19 footprint from micpie-88956-5204-52p-ruv-v to micpie-88956-5204-52p-ruv-v-za3 for ZA3 A-test SMT issues	
			PAGE20 : Change CN11 footprint from usb-020173mr004s555zl-4p-r-v to usb-020173mr004s555-4p-r-v-za3 for ZA3 A-test SMT issues	
			PAGE20 : Change CN14 footprint from usb-020173mr004s555zl-4p-r-v to usb-020173mr004s555-4p-r-v-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PJ2 footprint from dcjk-2dc3003-001211-5p to dcjk-2dc3003-001211-5p-v-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PR104 footprint from RC3720 to rc3720-0_8h for ZA3 A-test SMT issues	
			PAGE23 : Change PR112 footprint from RC3720 to rc3720-0_8h for ZA3 A-test SMT issues	
			PAGE14 : Change U9 footprint from QFN64-8X8-4-65P-0_85H to qfn64-8X8-4-65p-0_85h-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PU7 footprint from QFN28-5X5-5-33P to qfn28-5x5-5-33p-za3 for ZA3 A-test SMT issues	
			PAGE22 : Change U12 footprint from LQFP128-16X16-4 to lqfp128-16x16-4-za3 for ZA3 A-test SMT issues	
			PAGE23 : Change PJ1 footprint from bat-c144f8-108a1-l-8p-l-v-zg8 to bat-c144f8-108a1-l-8p-l-v-za3 for ZA3 A-test SMT issues	
			PAGE30 : Change HOLE8 HOLE9 HOLE10 footprint	
			PAGE16 : Modify SPK circuit	
		20090116	PAGE21 : Add CN8 PIN6 PIN7 to GND	
			PAGE30 : Modify HOLE8 HOLE9 HOLE10 symbol	
			PAGE21 : Change CN3 footprint from BL123-04R-4P-R-BL5 to 88513-0401-4p-r	
			PAGE21 : Change CN3 P/N	
		20090117	PAGE16 : Change CN7 P/N from DFHS04FS969 to DFHD04MRA75	
			PAGE4 : Change CN9 P/N from DFHS04FS969 to DFHD04MRA75	
		20090119	PAGE23 : stuff PR10 for Battery issues	
		20090121	PAGE22 : Modify SUSLED# from GPIO30 to GPIO40	
			PAGE27 : Change PL5 P/N from DC-33D5M000 to DC-2280M002	
		20090129	PAGE15 : Change C209 P/N from CH62202Z233 to CH52202MA91	
			PAGE15 : Change C209 footprint from CC1206 to CC0805	
			PAGE19 : Change CN18 P/N from DG052000031 to DFHS52FR025 for cost issues	
			PAGE19 : Change CN19 P/N from DG052000031 to DFHS52FR025 for cost issues	
			PAGE20 : Add R329 and C302 for EMI 48MHz issues	
			PAGE19 : Change C182 P/N from CH44702K912 to CH4472K9B00	
		20090205	PAGE8 : Add T60 T61 T62 T63 test point for Boundary Scan	
			PAGE4 : Modify JETC pins for Boundary Scan	
			PAGE9 : Modify JETC pins for Boundary Scan	
			PAGE16 : Modify CN7 pin5 pin6 for ESD issues	
			PAGE14 : Change CN10 P/N form DFWF20MS000 to DFWF20MS002	
			PAGE14 : Change CN10 footprint form 88442-2001-20p-luv to 87242-2001-20p-luv	
			PAGE8 : No stuff C160 for C6 issues	
		20090206	PAGE15: Add R255 for EMI request	

Model	REV	DATE	CHANGE LIST	NOTE
ZA3	B1A	20090206	PAGE16 : Reverse C301 R322 U19 R323 R324 for SPK AMP Power	ECN Release
		20090207	PAGE30 : Add C303 C304 C305 C306 C307 C308 for EMI Request	
			PAGE15 : No stuff R208 for EC not use BL_STATE rev.b 20090207	
			PAGE30 : C309 C310 for EMI Request	
			PAGE4 : Change R98 R87 R97 P/N from CS05102FB09 to CS05602JB17 rev.b 20090207	
			PAGE9 : Change R260 R259 R256 P/N from CS05102FB09 to CS05602JB17	
			PAGE9 : Change R257 P/N from CS02702JB21 to CS05602JB17 rev.b 20090207	
		20090209	PAGE8 : Change T60 T61 T62 T63 footprint from TP3075 to TP3050	
			PAGE8 : Modify HOLE10 HOLE5 HOLE7 footprint	
			PAGE15 : Change U8 P/N from AL005243000 to AL005243001	
	C1A	20090210	PAGE16 : Change R181 R176 P/N from CS07502FB17 to CS05102JB35	
			PAGE7 ~ PAGE12 : Change U15 P/N from AJSLGFQ0T02 to AJ0QV230T01	
		20090211	PAGE30 : C311 C312 for EMI Request	
			PAGE30 : Modify CN10 P/N and footprint for EMI request	
		20090212	PAGE16 : Change R204, R187, R313, R304 P/N from CS32003F933 to CS33603F911	
			PAGE17 : Change C4 C5 P/N from CH02706JB06 to CH03306JBD7 for vender suggest	
			PAGE3 : Change C42 C43 P/N from CH02706JB06 to CH03306JBD7 for vender suggest	
			PAGE18 : Change C250 C251 P/N from CH02206JB08 to CH02706JB06 for vender suggest	
		20090213	PAGE16 : Change R164 P/N from CS21002JB34 to CS22002JB02 for Ben check	
			PAGE16 : Change R167 P/N from CS00002JB38 to CS33602JB17 for Ben check	
		20090213	PAGE11 : Change C163 C136 connect SCH_VCCSUS3 power net	
		20090228	PAGE22 : Change U16 Pin5 from +3VPCU to +3V_S5	
			PAGE22 : Stuff D17, Reserve R262, Change C267 C270 connect from 3V_VDD_EC to +3V	
			PAGE6 : Modify R326 from 10K to 100K and pull up +3V and Change R168 from 10K to 100K	
		20090301	PAGE21 : Modify CN8 footprint and pin define	
			PAGE18 : Modify 8040 circuit to 88SA8052 add L22 R330 R331 R99 R339	
			PAGE4 : Modify R150 from CPU side to SCH side	
			PAGE4 : Change R88 P/N from CS05602JB17 to CS11202JB21	
			PAGE4 : Change R81 P/N from CS00002JB38 to CS02402JB11	
			PAGE6 : Change R100 R101 P/N from CS11002FB22 to CS11002JB32	
			PAGE13 : Add R112 R332 of RAM RST issues for intel suggest	
			PAGE15 : Change R215 P/N from CS41002JB20 to CS41002FB28	
			PAGE8 : Add R333 R334 R335 R336 for LPC AD0-AD3	
			PAGE8 : Change C233 C231 C243 C240 C239 C238 C237 C235 from SDVO chip side to SCH side	
			PAGE3 : Change R43 P/N from CS00002JB38 to CS31002JB28	
			PAGE9 : Change R186 R184 R309 R296 P/N from CS31002JB28 to CS21002JB34	
			PAGE9 : Del RN8 and Add R337 R338 to SCH SMBUS	
			PAGE15 : Modify R210 R23 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE16 : Modify R275 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE22 : Modify R138 R139 R207 R327 R328 R65 R82 R83 R92 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE10 : Modify R111 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE19 : Modify R160 R161 R162 R178 R179 R180 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE3 : Modify R39 R36 footprint from RC0402 to SHORT0402 for 0 ohm cost down	
			PAGE22 : Modify R110 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
			PAGE11 : Modify R126 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
			PAGE16 : Modify R144 R149 R170 R183 R246 R251 R197 R198 R199 R200 footprint from RC0603 to SHORT0603 for 0 ohm cost down	
	20090302		PAGE16 : Modify R168 P/N from CS31002JB28 to CS41002JB20	
			PAGE23 : Modify PJ1 footprint from bat-c144f8-108a1-l-8p-l-v-za3 to bat-c144f8-108a1-l-8p-l-v for SMT issues	
			PAGE14 : Add C313 C314 C315 for EMI issues	
	20090303		PAGE16 : Add R340 for EC PCBEEP	
			PAGE3 : Del R27 for CR DB +3VSUS issues	
			PAGE20 : Del R329 C302 for CR DB +3VSUS issues and modify CN5 pin12 to +3VSUS	
			PAGE6 : Add and revrse Q27 R329 for C6 circuit	
			PAGE19 : Add C318 for LPC issues	
			PAGE30 : Add C302 C316 C317 for EMI issues	
			PAGE13 : Del RN4 and Add R341 R342 for RAM issues	
			PAGE9 : Stuff R297 for SMI#	
			PAGE9 : No stuff R239 for SWI#	
			PAGE22 : Del D6 for SWI# issues	
	20090304		PAGE9 : Change R297 from +3V_S5 to +3V for SMI#	
			PAGE22 : Del SWI# net and Add test point T36	
			PAGE19 : No stuff C182 and change P/N from CH4472K9B00 to CH4471Z3B07	
	20090305		PAGE16 : Change U18 P/N from AL001453000 to AL001454001	
			PAGE19 : Change CN18 CN19 P/N from DFHS52FR025 to DG052000031	
			PAGE15 : Change CN1 P/N from DFHS30FR299 to DFHS30FR014 for SMT issues	